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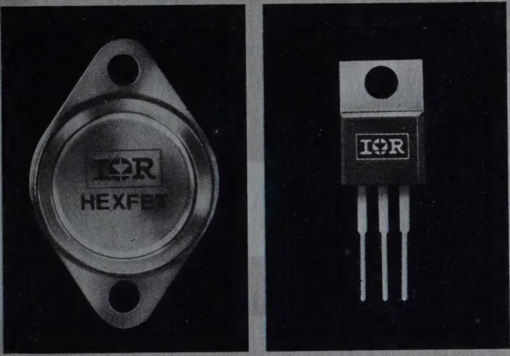

INTERNATIONAL RECTIFIER

HEXFET DATABOOK

POWER MOSFET APPLICATION AND PRODUCT DATA

INTERNATIONAL RECTIFIER

HEXFET™* DATABOOK

POWER MOSFET
APPLICATION AND PRODUCT DATA

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PREFACE

In mid-1979, International Rectifier introduced a new series of power MOSFETs to industry that opened vast, new opportunities for designers of any equipment, system or power supply that had, until that time, been limited by the performance characteristics of bipolar transistors.

International Rectifier's "HEXFET" technology, so named because of a structure based on thousands of hexagonal cells in densities up to 500,000 per square inch, brought the first MOSFETs to the power range capable of matching the on-resistance of bipolar transistors. For the first time, the advantages of power MOSFETs could be utilized without a sacrifice in efficiency.

This technological feat has sparked a revolution in design, capitalizing on the advantages of voltage control, extremely high switching speeds, temperature stability and the rugged physical characteristics of power MOSFETs. There are few circuits previously designed with bipolar transistors that cannot now be designed with MOSFETs to perform far better, in less space, with fewer components, and without the complexity of protective circuits required by the bipolar counterparts.

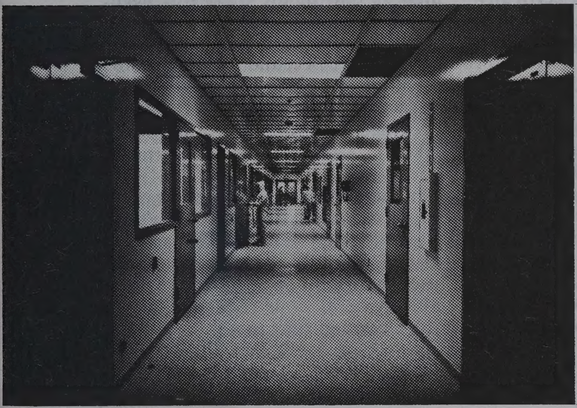
Along with this contribution to technology,

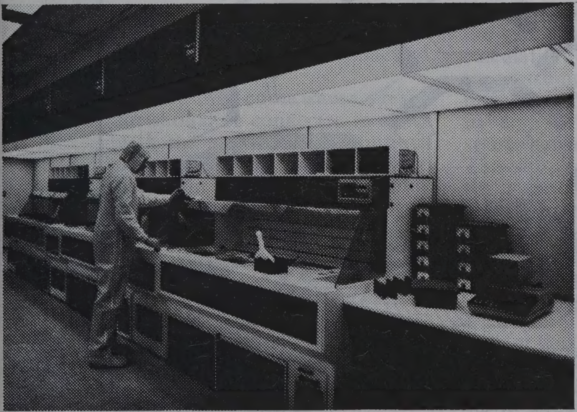
International Rectifier brought a commitment to power MOSFETs that has made the company today's leader in the field.

A commitment to quality. A commitment to production that enabled the company to ship more power MOSFETs in the 25-watt and above range than all other power MOSFET manufacturers in the world combined during 1980. A commitment to distribution that has put yesterday's laboratory achievement onto Distributors shelves around the world. Perhaps the most convincing proof of the total commitment International Rectifier has made is pictured below. This new structure houses today's largest state-of-the-art, high technology facility in the world devoted exclusively to power MOSFET wafer fabrication. On stream now, its initial production capacity is sufficient to supply the entire industry requirements for power MOSFETs in 1981, and is expandable to meet all demands to be experienced during the evolution from bipolar transistors to power MOSFETs in the equipment of tomorrow.

This DATABOOK lists todays broadest line of readily available power MOSFETs. More types and packages will follow to make your design job easier and your products better.

We're committed to that.





CHAPTER 1

APPLICATION NOTE 936

The Do's and Don'ts of Using Power HEXFETs™

By **BRIAN R. PELLY**, Vice President, Worldwide Applications Engineering

Summary

In common with all power semiconductor devices, power MOSFETs have their own technical subtleties, which must be properly understood if the designer is to get the most out of them. In this article, some of the most common "Do's and Don'ts" of using power HEXFETs are explained.

Introduction

Power HEXFETs offer many advantages over conventional bipolar transistors, in both linear and switching applications. These advantages include very fast switching, absence of second breakdown, wide safe operating area, and extremely high gain. Typical applications are high frequency switching power supplies, chopper and inverter systems for DC and AC motor speed control, high frequency generators for induction heating, ultrasonic generators, audio amplifiers, AM transmitters, computer peripherals, telecommunications equipment, and a host of special military and space needs.

There are several basic types of power MOSFETs available. Original designs used so-called V-groove or U-groove structures, while the trend today is towards vertical D-MOS technology, with a closed cellular source configuration. This technology was first embodied in the HEXFET structure, shown in Figure 1.

Current flows vertically through the silicon from the drain, through the body of the device, then horizontally through the channel region, and vertically out of the source, as illustrated. The flow of transistor current is controlled by the voltage applied between the gate and source terminals; the applied gate voltage sets up a field in the channel region, which modulates the resistance of the device. The gate is isolated electrically from the body; as a result, the power HEXFET has a very high, almost infinite, DC gain.

A feature of power MOSFETs is that they inherently have built into them an integral reverse body-drain diode. The existence of this diode is explained by reference to Figure 1. When the source terminal is made positive with respect to the drain, current can flow through the middle of the source cell, across a forward biased P-N junction. In the "reverse" direction, the power HEXFET thus behaves like a P-N junction rectifier.

The integral body-drain diode is a real circuit element, and its current handling capability is typically as high as that of the transistor itself. Some circuits require an "inverse" rectifier to be connected across the switching device, and in these circuits it will often be possible to utilize the body-drain diode of the HEXFET, provided the proper precautions are taken.

In this application note, some of the most common do's and don'ts of using power HEXFETs are described. The objective is to help the user get the most out of these remarkable devices, while reducing "on the job" learning time to a minimum.

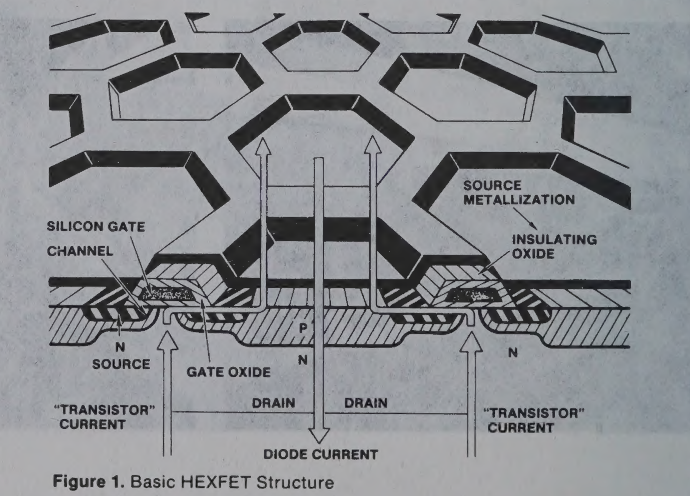


Figure 1. Basic HEXFET Structure

Be Careful When Handling & Testing Power HEXFETs

The user's first "contact" with the power HEXFET could be a package of parts arriving on his desk. Even at this stage, it behooves one to be knowledgeable about some elementary precautions.

Power HEXFETs, being MOS devices, can potentially be damaged by static charge when handling, testing or installing into a circuit. The problem is rather slight by comparison with that experienced with low level MOS devices. Power HEXFETs are, after all, *power* devices; as such, they have much greater input capacitance, and are much more able to absorb static charge without excessive build-up of voltage. In order to avoid possible problems, however, the following procedures should be followed as a matter of good practice, wherever possible:

- HEXFETs should be left in their anti-static shipping bags, or conductive foam, or they should be placed in metal containers or conductive tote bins, until required for testing or connection into a circuit. The person handling the device should ideally be grounded through a suitable wrist strap, though in reality this added precaution is seldom essential.
- HEXFETs should be handled by the package, not by the leads.

When checking the electrical characteristics of the power HEXFET on a curve tracer, or in a test circuit, the following precautions should be observed:

- Test stations should use electrically conductive floor and table mats that are grounded. Suitable mats are available commercially.
- When inserting HEXFETs into a curve tracer or a test circuit, voltage should not be applied until all terminals are solidly connected into the circuit.
- When using a curve tracer, a resistor should be connected in series with the gate to damp spurious oscillations that can otherwise occur on the trace. A suitable value of resistance is 100 ohms.
- For repeated testing, it is convenient to build this resistor into the test fixture.
- When switching from one test range to another, voltage and current settings should be reduced to zero, to avoid the generation of potentially destructive voltage surges during switching.

The next step is to connect the power HEXFET into an actual circuit. The following simple precautions should be observed:

- Work stations should use electrically grounded table and floor mats.
- Soldering irons *should be grounded.*

Now that the power HEXFET has been connected into its circuit, it is ready for the power to be applied. From here on, success in applying the device becomes a matter of the integrity of the circuit design, and of what circuit precautions have been taken to guard against unintentional abuse of the HEXFET's ratings.

The following are the interrelated device and circuit considerations that lead to reliable, trouble-free design.

Beware of Unexpected Gate-to-Source Voltage Spikes

Excessive voltage will punch through the gate-source oxide layer and result in permanent damage.

This seems obvious enough, but it is not so obvious that transient gate-to-source overvoltages can be generated that are quite unrelated to, and well in excess of, the amplitude of the applied drive signal. The problem is illustrated by reference to Figure 2.

If we assume that the impedance, Z, of the drive source is high, then any positive-going change of voltage applied across the drain and source terminals (caused, for example, by the switching of another device in the circuit) will be reflected as a positive-going voltage transient across the source and the drain terminals, in the approximate ratio of:

$$\frac{1}{1 + \frac{C_{gs}}{C_{dg}}}$$

The above ratio is typically about 1 to 6. This means that a change of drain-to-source voltage of 300V, for example, could produce a voltage transient approaching 50V between the gate and source terminals. This calculation is based upon the worst case assumption that the transient impedance of the drive circuit is high by comparison with the gate-to-source capacitance of the HEXFET. This situation can, in fact, be quite easily approximated if the gate drive circuit contains inductance — for example, the leakage inductance of an isolating drive transformer. This inductance exhibits a high impedance for short transients, and effectively decouples the gate from its drive circuit for the duration of the transient.

The positive-going gate-to-source voltage transient produced under the above circumstances is undesirable because it may exceed the gate voltage rating of the device, causing permanent damage; moreover, it tends to turn the device ON "unintention-

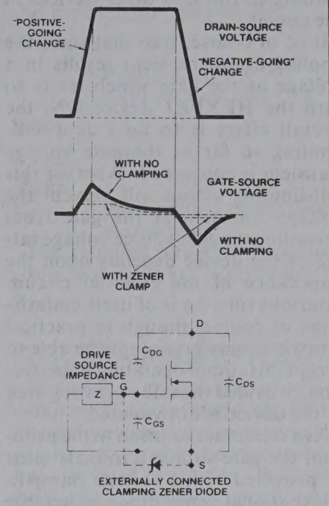


Figure 2. A Rapidly Changing Applied Drain-Source Voltage will Produce Gate-Source Voltage Transients

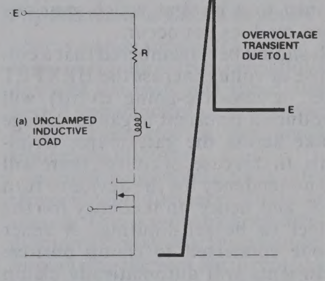


Figure 3. Drain-Source Overvoltage Transient when Switching Off with Unclamped Inductive Load

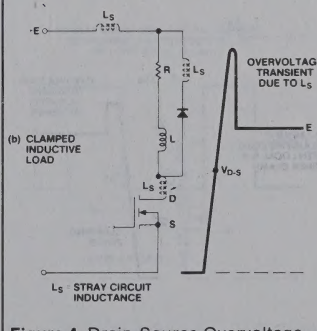

L_S
E
R
L_S
OVERVOLTAGE TRANSIENT DUE TO L_S
E
(b) CLAMPED INDUCTIVE LOAD
L
V_{D-S}
L_S
D
S
L_S = STRAY CIRCUIT INDUCTANCE

Figure 4. Drain-Source Overvoltage Transient Produced by Stray Circuit Inductance When Switching Off with Clamped Inductive Load

ally", causing transient current overloading of this and other devices in the circuit.

It is, of course, true that since the applied drain transient results in a voltage at the gate which tends to turn the HEXFET device ON, the overall effect is to an extent self-limiting so far as the gate voltage transient is concerned. Whether this self-limiting action will prevent the voltage transient at the gate from exceeding the gate-source voltage rating of the device depends upon the impedance of the external circuit. Spurious turn-on is of itself undesirable, of course, though in practical terms one may grudgingly be able to accept this circuit operating imperfection, provided the safe operating area of the device is not violated.

As a minimum solution to the problem, the gate-source terminals must be provided with a voltage clamp (a conventional zener diode is suitable for this purpose) to prevent the gate-source voltage rating from being exceeded. A more fundamental solution, of course, is to make the impedance of the gate circuit low enough that not only is the gate-source voltage rating not exceeded, but also the voltage transient at the gate is contained to a level at which spurious turn-on does not occur.

It should be remembered that a collapse of voltage across the HEXFET (i.e., a negative-going dv/dt) will produce a transient negative voltage spike across the gate-source terminals. In this case, of course, there will be no tendency for the device to turn ON, and hence no tendency for the effect to be self-limiting. A zener diode connected to clamp positive transients will automatically clamp negative-going transients, limiting them to the forward conduction voltage drop of the zener.

Beware of Drain-Source Voltage Spikes Induced by Switching

The uninitiated designer is often not aware that self-inflicted overvoltage transients can be produced when the device is switched OFF, even though the DC supply voltage for the drain circuit is well below the V_{DS} rating of the HEXFET.

Figure 3 shows how a voltage spike is produced when switching the device OFF, as a result of inductance in the circuit. The faster the HEXFET is switched, the higher the overvoltage will be. Inductance is always present to some extent in a practical circuit, and therefore, there is always danger of inducing overvoltage transients when switching OFF. Usually, of course, the main inductive component of the load will be "clamped", as shown in Figure 4. Stray circuit inductance still exists, however, and overvoltage transients will still be produced as a result — to say nothing of the fact that the clamping diode may not provide an instantaneous clamping action, due to its "forward recovery" characteristic.

The first approach to this problem is to minimize stray circuit inductance, by means of careful attention to circuit layout, to the point that whatever residual inductance is left in the circuit can be tolerated. If the device has an inductive energy rating, use can be made of this rating for this situation. Generally, however, such ratings do not yet exist for power HEXFETs, and a clamping device should be connected, physically as close as possible to the drain and source terminals, as shown in Figure 5. A conventional zener diode, or a "transorb" clamping device, are satisfactory for this purpose. An alternative clamping circuit is shown in Figure 6. The capacitor C is a reservoir capacitor and charges to a substantially constant voltage, while the resistor R is sized to dissipate the "clamping energy" while maintaining the desired voltage across the capacitor. The diode D must be chosen so that its forward recovery characteristic does not significantly spoil the transient clamping action of the circuit.

A simple RC snubber can also be used, as shown in Figure 7. Note, however, that an RC snubber not only limits the peak voltage, it also slows down the effective switching speed. In so doing, it absorbs energy during the whole of the switching period, not just at the end of it, as does a voltage clamp. A snubber is therefore less efficient than a true voltage clamping device.

Note that the highest voltage transient occurs when switching the highest level of current. The waveform of the voltage across the HEXFET should be checked with a high-speed oscilloscope at the full load condition to ensure that switching voltage transients are within safe limits.

Do Not Exceed the Peak Current Rating

All HEXFETs have a specified maximum peak current rating. This is conservatively set at a level that guarantees long-term reliability, and it should not be exceeded.

It is often overlooked that peak transient currents can be obtained in a practical circuit that are well in excess of the expected normal oper-

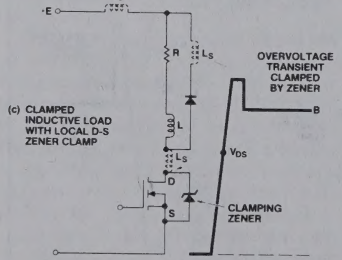

·E
Ls
R
Ls
OVERVOLTAGE TRANSIENT CLAMPED BY ZENER
B
(c) CLAMPED INDUCTIVE LOAD WITH LOCAL D-S ZENER CLAMP
L
Ls
VDS
D
S
CLAMPING ZENER

Figure 5. Overvoltage Transient at Switch-Off Clamped by Local Drain-Source Zener

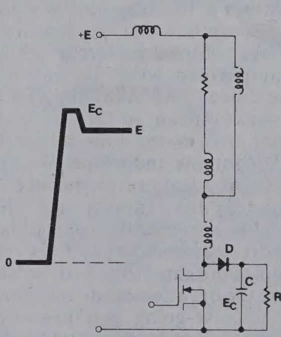


Figure 6. Overvoltage Transient at Switch-Off Limited by Local Diode-Capacitor-Resistor Clamp

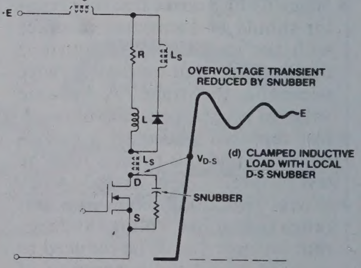

·E
Ls
R
Ls
OVERVOLTAGE TRANSIENT REDUCED BY SNUBBER
L
E
Ls
VD-S
(d) CLAMPED INDUCTIVE LOAD WITH LOCAL D-S SNUBBER
D
SNUBBER
S

Figure 7. Overvoltage Transient at Switch-Off Limited by Local Capacitor-Resistor Snubber

ating current, unless proper precautions are taken. Heating, lighting and motor loads, for example, consume high in-rush currents if not properly controlled. A technique that ensures that the peak current does not exceed the capability of the HEXFET is to use a current sensing control that switches OFF the HEXFET whenever the current instantaneously reaches a preset limit.

Unexpectedly high transient current can also be obtained as a result of rectifier reverse recovery, when a HEXFET is switched ON rapidly into a conducting rectifier. This is illustrated in Figure 8. The solution is to use a faster rectifier, or to slow down the switching of the HEXFET to limit the peak reverse recovery current of the rectifier.

Do Not Operate at an RMS Current In Excess of the Rating

All HEXFETs have a maximum continuous direct current rating, I_D. The internal bonding wires, bonding pads, and source metallization of the HEXFET are designed to carry this rated current continuously. The total continuous RMS current handled by the HEXFET should not exceed the I_D rating. This means that in a switching application, for example, if the peak current is I_{PK}, and the duty cycle is D, as illustrated in Figure 9, then the maximum permissible value of I_{PK} is $I_D/\sqrt{D}$, so long as this value is less than the $I_{D(max)}$ rating.

Stay Within the Thermal Limits

The power HEXFET, being a power device, is thermally limited. It must be mounted on a heatsink that is adequate to keep the junction temperature within the rated $T_{J(max)}$ (150° C) under the "worst case" condition of maximum power dissipation and maximum ambient temperature.

It must be remembered that in a switching application, the total power is due to the conduction loss and the switching loss. Switching time and hence switching losses are essentially independent of temperature, but the conduction losses increase with increasing temperature, because $R_{D(on)}$ increases with temperature. This must be taken into account when sizing the heatsink. The required thermal resistance of the heatsink can be calculated as follows:

The transistor conduction power, P_T, is given approximately by:

$$P_T = I^2_T\ R_{D(on)}\ [1 + 0.007\ (\Delta T_{JA} + T_A - 25)]$$

where I_T = RMS value of "transistor current"

$R_{D(on)}$ = ON resistance at 25° C

T_A = ambient temperature - °C

ΔT_{JA} = temperature rise, junction-to-ambient

The term within the brackets [ ] accounts for the typical 0.7% increase in $R_{D(on)}$ per degree C temperature rise above 25° C. The data sheet can be consulted for a more accurate value of temperature coefficient for any specific device.

The switching energy depends upon the voltage and current being switched and the type of load. The total switching loss, P_S, is the total switching energy, ϵ_T, multiplied by the operating frequency, f. ϵ_T is the sum of the energies due to the individual switchings that take place in each fundamental operating cycle.

$$P_S = \epsilon_T \cdot f$$

The total power dissipation is the sum of the conduction power, P_T, and the switching power, P_S.

$$P = P_T + P_S = I^2_T\ R_{D(on)}\ [1 + 0.007\ (\Delta T_{JA} + T_A - 25)] + P_S$$

Since:

$\Delta T_{JA} = PR_{JA}$

where:

R_{JA} = junction-to-ambient thermal resistance

The required value of R_{JA} for a given value of ΔT_{JA} is given by:

$$R_{JA} = \frac{\Delta T_{JA}}{I^2_T R_{D(on)}[1+0.007(\Delta T_{JA}+T_A-25)]+P_S}$$

The junction-to-ambient thermal resistance, R_{JA}, is made up of the internal junction-to-case thermal resistance, R_{JC}, plus the case-to-heatsink thermal resistance, R_{CS}, plus the sink-to-ambient thermal resistance, R_{SA}. The first two terms are fixed for the device, and the required thermal resistance of the heatsink, $R_{S\text{-}A}$, for a given junction temperature rise $\Delta T_{J\text{-}A}$, can be calculated from:

$$R_{S\text{-}A} = R_{J\text{-}A} - (R_{JC} + R_{C\text{-}S})$$

Pay Attention to Circuit Layout

Stray inductance in the circuit can cause overvoltage transients, slowing down of the switching speed, unexpected unbalance of current between parallel connected devices, and unwanted oscillations.

In order to minimize these effects, stray circuit inductance must be minimized. This is done by keeping conduction paths as short as possible, by minimizing the area of current loops, by using twisted pairs of leads, and

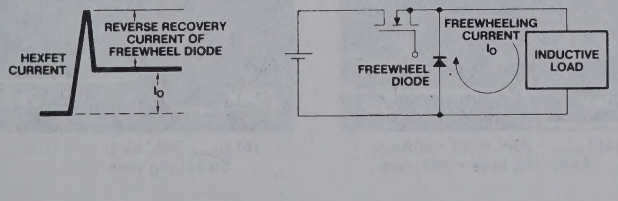


Figure 8. Switching on the HEXFET into a Conducting Rectifier Can Result in High Peak Current, due to Reverse Recovery of Rectifier.

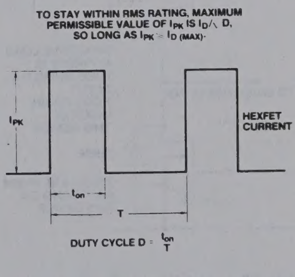

TO STAY WITHIN RMS RATING, MAXIMUM PERMISSIBLE VALUE OF I_{PK} IS $I_D/\sqrt{D}$, SO LONG AS $I_{PK} \leq I_{D\ (MAX)}$.
I_{PK}
HEXFET CURRENT
t_{on}
T
DUTY CYCLE D = $\frac{t_{on}}{T}$

Figure 9. To Stay Within I_D RMS Rating, Maximum Permissible Value of I_{PK} is $I_D/\sqrt{D}$, so long as $I_{PK} \leqslant I_{D(max)}$.

by using ground plane construction. Local decoupling capacitors alleviate the affects of any residual circuit inductance, once these measures have been taken.

Circuit layout should be kept as symmetrical as possible in order to maintain balanced currents in parallel connected HEXFETs. The gates of parallel connected devices should be decoupled by small ferrite beads placed over the gate connections, or by individual resistors in series with each gate. These measures prevent parasitic oscillations.

Be Careful When Using the Integral Body-Drain Diode

The HEXFET's integral body-drain diode exhibits minority carrier reverse recovery. Reverse recovery presents a potential problem when switching any rectifier off; the slower the rectifier, the greater the problem. The HEXFET's rectifier is relatively fast — not as fast as the fastest discrete rectifiers available, but considerably faster than comparably related conventional general purpose rectifiers. By comparison with the HEXFET itself, on the other hand, the switching speed of the integral reverse rectifier is quite slow. The switching speed of a circuit which utilizes the body-drain diode of the HEXFET may therefore be limited by the rectifier. Whether this will be so depends upon the circuit and the operating conditions.

The most common applications of the HEXFET in which the switching speed, and hence frequency, will potentially be limited by the rectifier, are DC to DC choppers, and inverters for regulated power supplies, electric motor controllers, and so on, in which "multiple" voltage pulses are used. Fortunately, these applications generally do not require ultra-fast switching, and hence they can tolerate the reverse recovery characteristic of the rectifier.

Regardless of the overall circuit configuration, or the particular application, the "local" circuit operating situation that is troublesome occurs when the freewheeling current from an inductive load is commutated from the integral rectifier of one HEXFET to the transistor of an "opposite" HEXFET, the two devices forming a tandem series connected pair across a low impedance voltage source, as shown in Figure 10. This "local" circuit configuration occurs in most chopper and inverter schemes.

If the incoming HEXFET switches ON too rapidly, the peak reverse recovery current of the integral body-drain diode of the opposite HEXFET will rise too rapidly, the peak reverse recovery current rating will be exceeded, and the device may possibly be destroyed.

The peak reverse recovery current of the rectifier can be reduced by slowing down the rate of change of current during the commutation process. The rate of change of current can be controlled by purposefully slowing down the rate of rise of the gate driving pulse. Using this technique, the peak current can be reduced to almost any desired extent, at the expense of prolonging the high dissipation switching period. The oscillograms in Figure 11 illustrate the effect. By slowing the total switch-ON time from 300ns to 1.8μs, the peak current of the IRF330 has been decreased from 20A to 10A. The energy dissipation associated with the "unrestrained" switch-ON in Figure 11(a) is 0.9mJ, whereas it is 2.7mJ for the controlled switch-ON of Figure 11(b). Note, however, that the average switching losses at a switching frequency of, say 5kHz, are quite manageable — 4.5W and 13.5W for Figures 11(a) and 11(b), respectively.

Note also that it is not necessary to slow the switching-OFF of the HEXFET, hence the energy dissipation at switch-OFF will be relatively small by comparison with that at switch-ON. For operation at frequencies up to a few kHz, where ultra-fast switching is not mandatory, slowing the applied gate drive signal to reduce the peak reverse recovery current of the "opposite" rectifier offers a good practical solution.

Be On Your Guard When Comparing Current Ratings

The user can be forgiven if he assumes that the continuous drain current rating, I_D, that appears on the data sheet represents the current at which the device can actually be operated continuously in a practical system. To be sure, that's what it should represent; unfortunately it often does not.

Most manufacturers assign a "continuous" current rating to the device which in practical terms cannot be used, because the resulting conduction power dissipation would be so large as to require a heatsink with an impractically low thermal resistance, and/or an impractically low ambient operating temperature.

Table 1 is an illustration of the present lack of standardization of current ratings amongst different MOSFET manufacturers. The devices with higher ON-resistance are seen to have generally higher current ratings assigned to them than the lower ON-resistance parts — a tra-

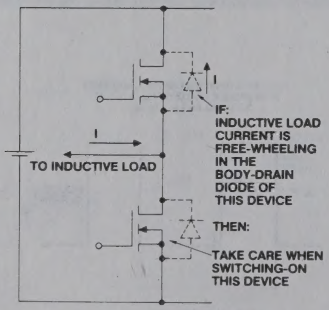
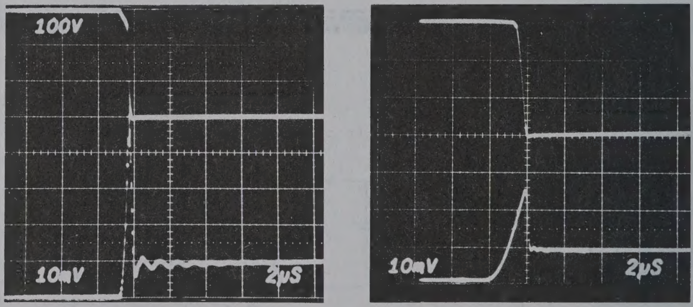


Figure 10. Local Circuit Configuration and Operating Condition Requiring Special Care When Using the HEXFET's Integral Body-Drain Diode.



(a) $I_{(max)}$ = 20A, di/dt = 50A/μs. Switching time = 300 nsec.

(b) $I_{(max)}$ 20A, di/dt = 50A/μs. Switching time 1.8μs.

Figure 11. Oscillograms of IRF330 Switching into Reverse Rectifier of Another IRF330 with Freewheeling Current of 4A.
Top Trace: Voltage 100V/div.
Bottom Trace: Current 4A/div.
Time Scale: 2μs/div.

vesty of the "correct" situation that would, and should, exist if all types of given chip size and junction-to-case thermal resistance were rated on the basis of a given power dissipation.

The best advice to the user is to compare different types *on the basis of ON-resistance,* and not of I_D rating. Fortunately, all manufacturers specify $R_{D(on)}$ at 25° C, and this provides a common basis for comparison. This parameter, taken in conjunction with the junction-case thermal resistance (which, unfortunately, not all manufacturers specify), is a much better indication of the HEXFET's true current handling capability.

Table 1. Comparison of Different Manufacturers' Practices for Assigning Current Ratings (All Parts are Rated 400V)

Device Type	$R_{D(on)}$ Ohms	I_D Amps	$R\theta_{J-C}$ °C/W	Calculated $T_{C(max)}$ Applicable to I_D °C
IRF330	1.0	4	1.67	90
MTP565	1.5	5	1.67	25
HPWR6504	1.0	5	1.39	80
VN4001A	1.5	8	?	<25 ?
VN0340B1	1.5	8	?	<25 ?

Conclusions

Power HEXFETs have many advantages. When properly applied they yield an overall system design that frequently has fewer components, is lighter and more compact, and has better performance than can be obtained with other types of devices.

In common with all power semiconductors, power HEXFETs do have their own little technical subtleties. If these subtleties are properly understood, the potential pitfalls can be easily overcome, at minimal cost — and potentially great reward. ☐

CHAPTER 2
APPLICATION NOTE 930

Applying International Rectifier's Power MOSFETs

By BRIAN R. PELLY, Vice President, World-wide Applications Engineering

International Rectifier's Power MOSFETs open the door to the design of advanced products by offering the superior characteristics of Field Effect Transistors at true high power levels. Power MOSFETs simplify circuitry because they are voltage-controlled devices and require only very small instantaneous currents from the signal source. They achieve switching times of less than 100 nanoseconds at high current levels. They have great ruggedness because of the absence of the second breakdown failure mechanism of bipolar transistors. In parallel operation they inherently "current share" rather than "current hog." The stability of the gain and response time characteristics over a wide temperature range is outstanding. The net result is a radically advanced power transistor of universal application capability.

HEXFET™ Technology

International Rectifier now offers a truly advanced line of power MOSFETs termed the HEXFETs™. The HEXFETs are IR's second generation power MOSFET design and feature uniquely advanced technology. The HEXFET technology achieves both new high power records in switching ratings for field effect transistors and new economies in MOSFET production costs. IR's

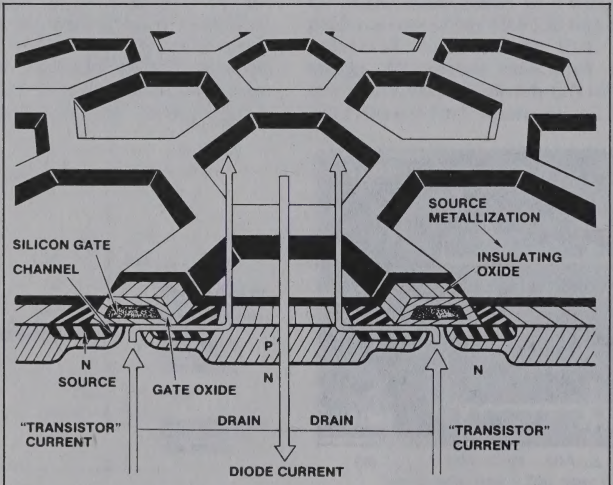
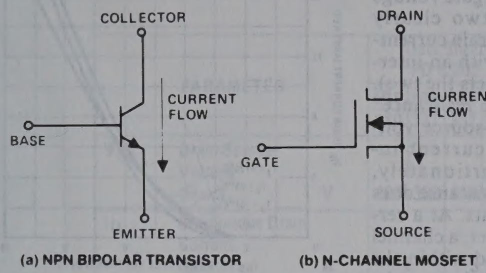


Figure 1. Basic HEXFET Structure

The HEXFET Structure

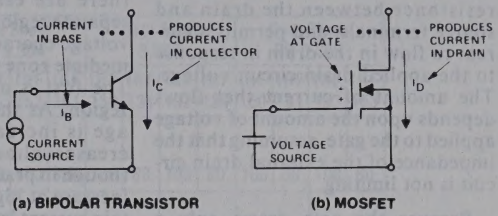
The HEXFET surface is characterized by a multiplicity of closed hexagonal source cells (over 500,000 per square inch) from which the name HEXFET is derived. In cross section, the HEXFET is based on a double-diffused (DMOS) structure. A channel is formed by double diffusion at the periphery of each hexagonal source cell. An insulating gate oxide layer covers the channel. A silicon gate then overlays both the insulating oxide and channel. The silicon gate in turn is insulated from the source by an additional oxide layer. All of the hexagonal source cells are then parallel connected by a continuous sheet of metalization which forms the source terminal.

Transistor action occurs by penetration of an electric field into the channel area which modulates the conductivity between drain and source. Conventional current flow is from the drain substrate, across the channel surface, and vertically out the source terminal.



(a) NPN BIPOLAR TRANSISTOR (b) N-CHANNEL MOSFET

Figure 2. Electrical Symbols for Bipolar and MOSFET



(a) BIPOLAR TRANSISTOR (b) MOSFET

Figure 3. Bipolar Transistor is Current-Driven, MOSFET is Voltage-Driven

HEXFETs set the stage for large scale usage in applications which previously could be handled only by the bipolar technology.

Until recently, large-area MOSFET devices combining the low on-resistance and the high-voltage characteristics of a true power transistor could not be fabricated. With IR's HEXFET technology, however, on-resistances as low as 0.05 ohms are possible at the 100 volt level. Voltage ratings as high as 500 volts are possible by making a tradeoff with higher on-resistance. HEXFET switching ratings in excess of 4 kilowatts are available in a single device.

The HEXFET Structure

As implied, the HEXFET structure involves a hexagonal device geometry. At the core is a radically new hexagonal cellular structure, illustrated diagrammatically in Figure 1. It is this hexagonal geometry, along with advanced MOS processing, that gives the HEXFET an on state resistance, $R_{DS(on)}$, one-third of that possible with the best previous MOSFET technology, in a given die size. At a given current level, therefore, the HEXFET can achieve a forward voltage drop quite comparable to the collector-emitter saturation voltage of high performance bipolar transistors that have about the same die size.

A planar, non V-groove structure, the HEXFET conducts current vertically. For high packing density, it uses a silicon-gate structure. The density of the hexagonal source cells on the top surface of the silicon die is over half a million cells per square inch. Electrons flow from a source cell through the channel which is around the periphery of that cell and then into the drain body. The bottom surface of the drain body is in electrical and thermal contact with the header.

The efficient hexagonal source pattern, the silicon gate, and advanced MOS processing techniques all combine to produce the HEXFETs' unique performance characteristics.

Some Basic Considerations

As we have seen, the HEXFET is IR's advanced design of power MOSFET. Power MOSFETs are majority carrier semiconductor devices, and their construction and principles of operation are fundamentally different from those of traditional bipolar transistors, which are minority carrier semiconductors. These fundamental differences must be understood if full advantage is to be taken of the MOSFETs' special performance features.

MOSFET Symbol and Terminology

The collector, base and emitter terminology for the terminals of a bipolar transistor is replaced by drain, gate, and source, respectively for a MOSFET. Figure 2 shows the circuit symbol for an N-channel MOSFET, and makes a comparison with a conventional bipolar transistor.

Driving the Power MOSFET

The conventional bipolar transistor is essentially a current-driven device. As illustrated in Figure 3 (a), a current must be applied between the base and emitter terminals to produce a flow of current in the collector. The amount of drive required to produce a given output depends upon the gain, but invariably a current must be made to flow into the base terminal to produce a flow of current in the collector.

The MOSFET is fundamentally different; it is a voltage-controlled device. A voltage must be applied between the gate and source terminals to produce a flow of current in the drain, as illustrated in Figure 3(b). The gate is isolated electrically from the source by a layer of silicon oxide. Theoretically no current flows into the gate when a DC voltage is applied to it — though in practice there will be an extremely small leakage current, in the order of nanoamperes.

With no voltage applied between the gate and source electrodes, the impedance between the drain and source terminals is very high, and only a small leakage current flows in the drain until the applied voltage exceeds the drain-to-source avalanche voltage. This is illustrated in Figure 4.

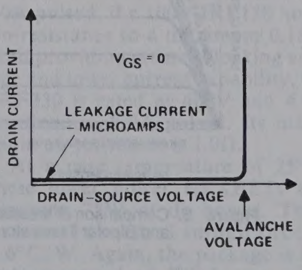


Figure 4. Drain-Source Blocking Characteristic

When a voltage is applied between the gate and source terminals, an electric field is set up within the MOSFET. This field modulates the resistance between the drain and source terminals, and permits a current to flow in the drain in response to the applied drain circuit voltage. The amount of current that flows depends upon the amount of voltage applied to the gate, assuming that the impedance of the external drain circuit is not limiting.

Because the gate draws only a minute DC leakage current, the DC current gain is extremely high, typically in the order of 10^9. In fact, this is a rather meaningless parameter for a power MOSFET, and it is not normally used. Because a flow of *current* in the drain is produced essentially by a *voltage* applied to the gate, a more useful parameter for the MOSFET is the *transconductance.* This is the change of drain current brought about by a 1 volt change of gate voltage.

The extremely low drive current requirement of the power MOSFET, and the associated extremely high power gain, are a major advantage over the conventional bipolar transistor or Darlington. This feature will often make it possible to drive the power MOSFET directly from CMOS or TTL integrated circuit logic.

The Static Operating Characteristics

The fundamental drain-source operating characteristics of the power MOSFET are illustrated in Figure 5(a). For comparison, Figure 5(b) shows the corresponding collector-emitter characteristics for a conventional bipolar transistor.

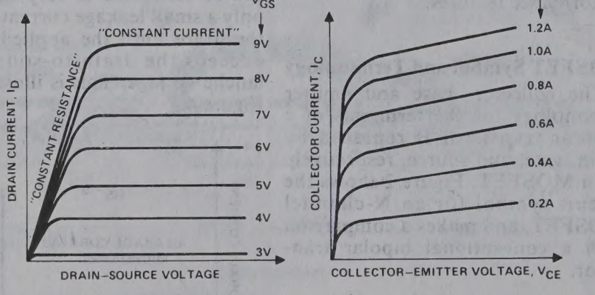
For any given value of gate voltage there are essentially two clearly separate regions on the drain current-voltage characteristic (with an intermediate zone that connects the two). The first is a "constant resistance" region. As the drain-to-source voltage is increased, the current increases almost proportionately, though in practice the resistance does increase at higher currents. At a certain current level, however, a channel pinchoff effect is reached within the device, and the operating characteristic moves into a constant current region.

The bipolar transistor also exhibits a generally similar type of collector characteristic. It does not, however, show a truly resistive effect in its saturation region, nor does it exhibit nearly such a well regulated constant current characteristic.

For switching applications, the On-Resistance $R_{DS(ON)}$ of the power MOSFET is obviously an important characteristic because it determines the power loss for a given drain current. The lower the On-Resistance the higher the current handling capability of the device. On-Resistance is thus an important "figure of merit" of the power MOSFET.

Threshold Voltage and Transconductance

Inspection of the static drain-source operating characteristics of Figure 5 reveals that as the gate-to-source voltage is increased from zero, initially the drain current does not increase significantly. Only once a certain threshold gate voltage has been reached, does the drain current start to increase appreciably.



(a) POWER MOSFET

(b) BIPOLAR POWER TRANSISTOR

Figure 5. Comparison of Idealized Output Characteristics of Power MOSFET and Bipolar Transistor

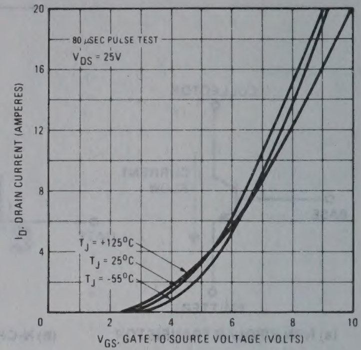


Figure 6. Transfer Characteristics (IRF130)

This is illustrated more clearly by the typical relationships between drain current and gate voltage shown in Figure 6. It is seen that in the operating region beyond the threshold gate voltage, the relationship between the drain current and the gate voltage is approximately linear. Stated another way, the rate of change of drain current with gate voltage — the transconductance referred to earlier — becomes relatively constant at higher values of drain current.

Features of IR Power MOSFETs

Basic Characteristics

Table 1 shows the available types at the time of publication of this article, September, 1979. Other types will continue to be introduced, and the reader should check with IR for the latest product information.

All IR's MOSFETs will conduct their rated continuous drain current, I_D, with less than 10 volts, V_{GS}, applied from gate-to-source. Conduction will begin before 3 volts $V_{GS(th)}$, threshold voltage is applied to the gate. The threshold voltage is always greater than 1 volt, which allows leakage currents from a previous stage to be easily bypassed to ground. A cutoff condition of the power stage is thereby assured without any special reverse-biasing. All units have a maximum junction operating temperature of 150°C.

Rated at 100V, 28A continuous and 70A pulsed, the IRF150 (Table 1) brings on-resistance down to the lowest value to date of any power MOSFET — 0.055Ω maximum. Typical on-resistance, just 0.04Ω, produces a 1.0V saturation-voltage drop

PARAMETER			Data Sheet PD 9.302				Data Sheet PD 9.304				Data Sheet 9.303				Data Sheet PD 9.305			
			IRF 330	IRF 331	IRF 332	IRF 333	IRF 350	IRF 351	IRF 352	IRF 353	IRF 130	IRF 131	IRF 132	IRF 133	IRF 150	IRF 151	IRF 152	IRF 153
V_{DS}	Drain-Source Voltage (Max.)	V	400	350	400	350	400	350	400	350	100	60	100	60	100	60	100	60
I_D	Continuous Drain Current (Max.)	A	4		3.5		11		10		12		10		28		24	
I_{DM}	Pulsed Drain Current (Max.)	A	8		7		25		20		30		25		70		60	
$R_{DS(on)}$	On-State Resistance (Max.)	Ohms	1		1.5		0.3		0.4		0.18		0.25		0.055		0.08	
P_D	Power Dissipation (Max.)	W	75				150				75				150			
g_{fs}	Forward Transconductance (Typical)	Mhos	3.5				9				5				10			
$t_{d(on)}$	Turn on Delay Time (Typical)	ns	50				60				50				60			
t_r	Rise Time (Typical)	ns	100				150				150				200			
$t_{d(off)}$	Turn off delay time (Typical)	ns	100				400				100				300			
t_f	Fall time (Typical)	ns	100				150				150				200			
C_{iss}	Input Capacitance (Max.)	pF	1000				4000				1000				4000			

Table 1. Ratings and Characteristics of IR's High Current HEXFETs. September 1979

at 25A, which is low enough to compare with the $V_{VE(SAT)}$ of a bipolar transistor of similar size, and lower than that of a Darlington transistor.

Such a small forward voltage drop is particularly impressive in light of the fact that the HEXFET requires only nanoamperes of gate drive, not the amperes of base drive a bipolar needs. In addition, the MOSFET does not suffer the loss of switching speed the bipolar does when driven hard into saturation.

The IRF350 (Table 1) is a high voltage version of the die size used for the IRF150 transistor. Rated at 400V and 11A continuous, 25A pulsed, the IRF350 has a maximum on-resistance of 0.30Ω. Moreover, an ability to switch 4.4kW continuously makes the IRF350 by far the highest-power MOSFET available anywhere in the world at the time of writing.

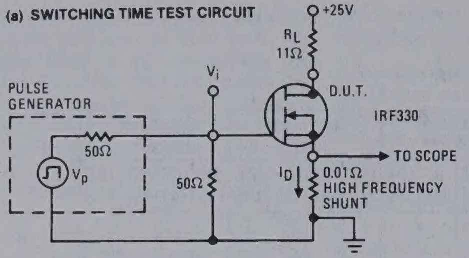
At a case temperature of 25°C, both of these HEXFETs have a continuous dissipation rating of 150W. Thermal impedance, from junction to case, is 0.83°C/W. Both the IRF150 and IRF350 families are in standard TO-3 metal cases, with copper base and 0.06in. diameter pins for high electrical and thermal conductivity.

The lower power IRF130 and IRF330 families provide voltage ratings and maximum on-resistance values essentially equivalent to the first generation IRF100 and IRF300 MOSFET families (now obsolescent). The HEXFETs accomplish the specifications with a transistor die about one-third the size of the original MOSFET types.

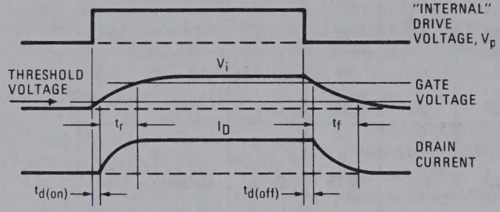
Able to handle 12A continuous, 30A pulsed, the 100V IRF130 holds on-resistance to a maximum 0.18Ω. And providing greater blocking voltage and lower current capability, the IRF330 is rated at 400V and 4.0A continuous, 8.0A pulsed. Its maximum on-resistance is 1.0Ω.

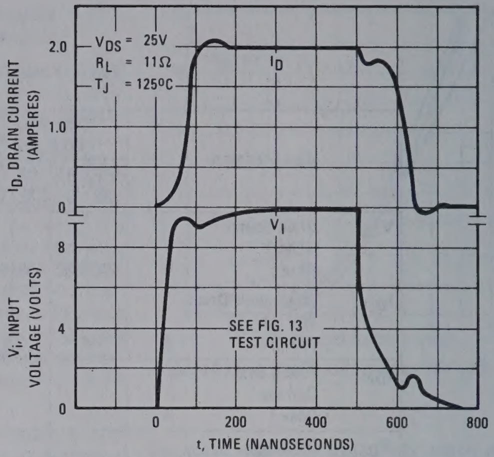
At a case temperature of 25°C, these lower power HEXFETs can dissipate 75W of dc power. Their internal thermal impedance is 1.6°C/W. Again, the package is the industry-standard TO-3 case, with 0.04in diameter pins.

(a) SWITCHING TIME TEST CIRCUIT



(b) THEORETICAL SWITCHING WAVEFORMS





(c) TYPICAL ACTUAL SWITCHING WAVEFORMS

Figure 7. Switching the MOSFET

Switching Times

MOSFET power transistors are much faster than bipolar power transistors of comparable size, primarily because they do not have minority carrier delay times. The response times of MOSFETs are determined primarily by the device capacitances, and secondarily by such factors as the extremely short channel transit time of the electrons.

The input capacitance, C_{iss}, is the primary factor which determines the response time of a MOSFET. Although MOSFETs can be controlled by extremely low currents (i.e. high source impedances), the relatively long charge and discharge time of the input capacitance, C_{iss}, results in a tradeoff of response time against extreme sensitivity. A first order approximation of the response time of a MOSFET can be made by determining the time constant which results from the input capacitance times the effective source impedance.

Figure 7 shows typical switching waveforms of an IRF330 when driven by a 500 nanosecond-wide pulse. A good first order understanding of the switching response times $t_{d(on)}$, t_r, $t_{d(off)}$, and t_f, can be made by considering the power MOSFET an ideal switch with a 3 volt "on" threshold. The output current can be considered controlled, without delay, by the instantaneous gate voltage which, in turn, is controlled by the time constant formed by R_{input} x C_{iss}.

With these concepts in mind, the switching waveshapes of Figure 7(b) and the response times can be more easily understood. The turn-on delay, $t_{d(on)}$, is primarily the time for the transistor gate capacitance to be charged by the control signal to the threshold level of 3 volts maximum. The rise time, t_r, is the gate charging time required to drive from the threshold voltage, through the linear control region, to the gate voltage (typically 5 to 8 volts) required for full conduction of the drain current. In turn-off the procedure is reversed, and the turn-off delay time, $t_{d(off)}$, is primarily the time required for the gate capacitance to discharge from the gate overdrive saturation voltage (typically 10 volts) to the active gate control region (typically 5 to 8 volts). Finally, the fall time, t_f, is primarily the time delay required for the input capacitance to discharge through the active control region to the gate threshold voltage.

Figure 8 shows typical relationships for the IRF330 between the amplitude of the applied gate voltage signal, the turn off delay time, the fall time, and the rise time of the drain current, with the simple "resistive" gate drive circuit shown in Figure 7. Note that the turn off delay time increases with increasing gate drive, for the reasons already explained. The rise time of the drain current, on the other hand, decreases with increasing gate drive; this is because the higher the applied gate drive signal the faster the gate to source voltage reaches the level needed to support the drain current. The fall time of the drain current remains practically constant with applied gate drive; this is because the decay of the gate-to-source voltage below the point at which the drain current I_D can no longer be maintained, is practically independent of the amplitude of the applied gate signal.

Typical relationships between switching times and gate circuit re-

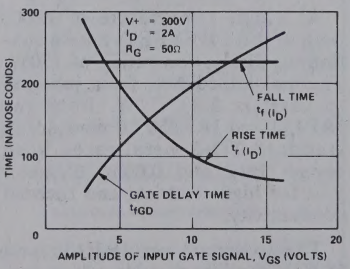


Figure 8. Typical relationships between Switching Times and Applied Gate Voltage (IRF330)

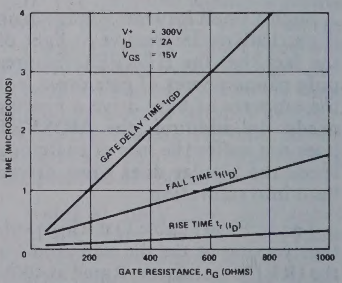


Figure 9. Typical relationships between Switching Times and Gate Circuit Resistance (IRF330)

sistance are shown in Figure 9. Predictably, the higher the gate resistance, the longer the switching times, because of the longer time constant R_G C_{iss}.

Simple Capacitive Speed-Up Circuit

The alert designer will realise that circuit techniques for forcing the charge on C_{iss}, give a means of controlling the response time of the MOSFET, or alternatively the input impedance level at which a given response time occurs.

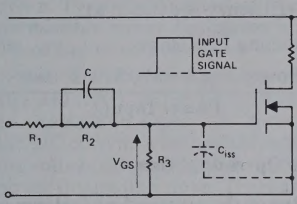


Figure 10. Gate Speed-up Circuit

Figure 10 shows a simple gate "speed-up" circuit. The circuit produces a significant reduction in the switching times, at the expense of the need for an increased amplitude of input gate signal, and an increased, (but still comparatively low) current drain on the drive source. When switching on, the capacitor C initially provides a low impedance path for the applied gate pulse, bypassing the resistor R_2, and thus the input capacitance C_{iss} of the MOSFET is rapidly charged. When switching off, the capacitor C is charged positively on its left-hand terminal; the charged capacitor forces a discharge current through the input capacitance of the MOSFET, thus making it switch off rapidly.

A point to remember about this gate speed-up circuit is that to be effective it does require an increase in the amplitude of the source signal voltage, because of the voltage dividing effect of R_3 with R_1 and R_2. Another point is that the resistor R_3 draws a continuous current from the gate drive source. Clearly it is desirable that the value of R_3 should be as high as possible. Figure 11 shows typical switching times for different values of R_3, for a given values of R_1, R_2 and C. It is seen that very fast switching times — in the order of 50 nanoseconds — can be obtained with the gate-to-source resistance R_3 as high as 10k Ohms. This represents a continuous current drain on the gate drive source of about 1mA. This is an order of magnitude lower than the drive current required for a comparably rated bipolar Darlington, which in any event exhibits switching times more than an order of magnitude longer.

Figure 12 shows typical relationships between the switching speeds of the IRF330 and the drain current, with and without a gate speed-up circuit. Note the drastic reduction in the turn off delay and fall times with the speed-up circuit, at drain current levels above 1A. The increase in the fall time at low levels of drain current is due to the drain-to-source capacitance, C_{oss}. The lower the drain current, the higher the load resistance R, and the greater the time constant RC_{oss}. A typical relationship between C_{oss} and drain to source voltage is shown in Figure 13.

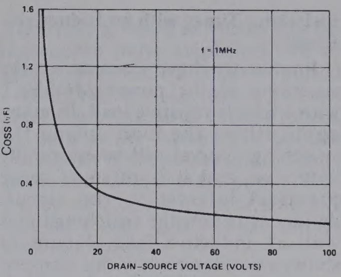


Figure 13. Typical relationships between Drain-Source Voltage and Drain-Source Self Capacitance (IRF330)

Simple external circuit techniques such as this can be used to obtain the fast switching speeds possible with power MOSFETs, yet maintain extremely high effective gain, thereby keeping complexity to a minimum. Power MOSFETs operating at many amperes and kilowatt power levels can commonly be driven directly from linear and digital IC components, whilst switching times still much faster than those of bipolar power transistors are easily achieved.

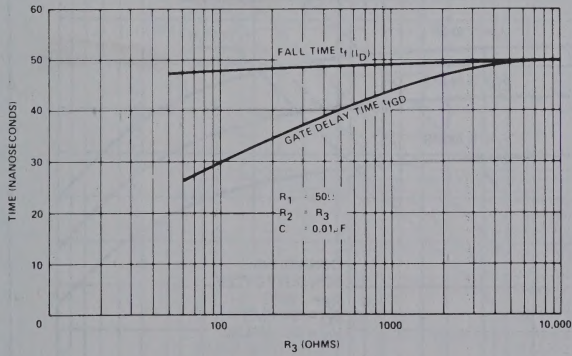


Figure 11. Values in Gate Speed-up Circuit and Switching Times (IRF330)

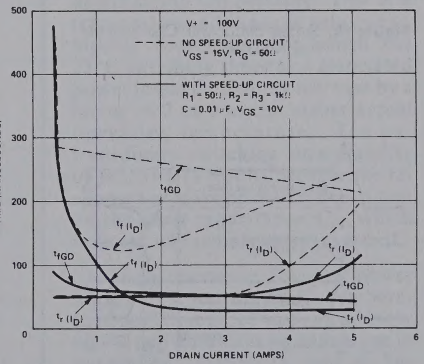


Figure 12. Typical relationships between Switching Times and Drain Current with and without Gate Speed-up Circuit (IRF330)

Switching Times with an Inductive Load

So far we have considered the switching of the power MOSFET with a simple resistive load. In many applications the load during the switching interval will be essentially inductive, and it is often of more practical interest to the circuit designer to know the switching times with an inductive load. Figure 14 shows a simple circuit with a clamped inductive load; corresponding idealized switching waveforms are shown in Figure 15. Note that at switch-on the current first rises, then the voltage falls. At switch off the drain voltage rises, then the current falls. Note that this assumes that the load is sufficiently inductive that current flows continuously in it; through the MOSFET when it is switched on, and through the clamping diode when the MOSFET is switched off. It is also assumed that stray circuit inductance between the clamping diode and the MOSFET is negligible. Thus at switch on, load current that is already flowing in the clamping diode commutates into the MOSFET, and the transfer of this current is unrestricted by stray circuit inductance. In general this assumption for the switch on condition is somewhat pessimistic, but it can be approximated in certain circuits.

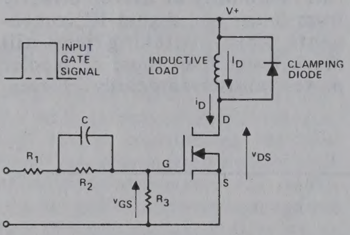


Figure 14. Simple circuit with Clamped Inductive Load

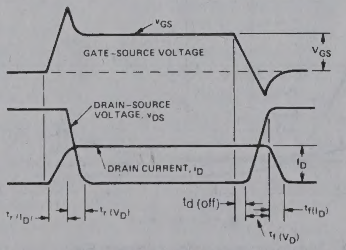


Figure 15. Idealized Switching Waveforms for Clamped Inductive Load

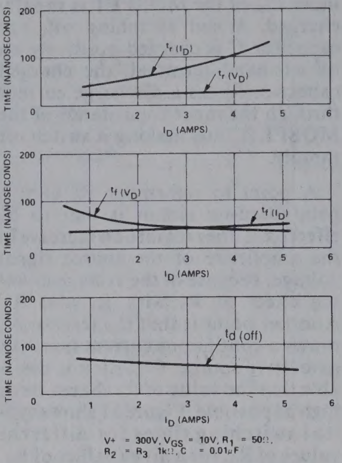


Figure 16. Typical relationships between Switching Times and Drain Current with Clamped Inductive Load and Gate Speed-up Circuit (IRF330)

Figure 16 shows typical relationships between the switching times and the drain current for a clamped inductive load with a gate speed-up circuit.

Maximum Operating Frequency

Because the switching times of the power MOSFET are very fast — at least an order of magnitude faster than those of comparably rated bipolar transistors — the energy dissipated during switching is very much lower, and the power MOSFET is able to operate at switching frequencies an order of magnitude or more higher.

Relationships between operating frequency and switching efficiency of the IRF330 power MOSFET with a resistive load, are shown in Figure 17. This data is based upon actual measured values of switching energy at a supply voltage of 300V, and a 50% duty cycle. Figure 17 takes account of the losses in the power MOSFET itself, and not of other components in the circuit; it does not therefore represent the overall circuit efficiency. Clearly, so far as the MOSFET itself is concerned, switching frequencies up to 500kHz or higher are quite feasible. The switching efficiency is defined as:

$$\text{Switching Efficiency} = \frac{\text{Power Input} - \text{MOSFET losses}}{\text{Power Input.}}$$

Safe Operating Area

One of the outstanding features of IR's power MOSFETs is that they do not display the second breakdown phenomenon which is frequently the Achilles heel of bipolar transistors. A simple physical explanation accounts for this superiority. If localized, potentially destructive, heating occurs within a MOSFET transistor, the carrier mobility in that area decreases. As a result the MOSFET has a positive temperature coefficient and acts in a self-protective manner by forcing currents to be uniformly distributed through the silicon die. In contrast a bipolar transistor, particularly under conditions of high collector-emitter voltage, displays

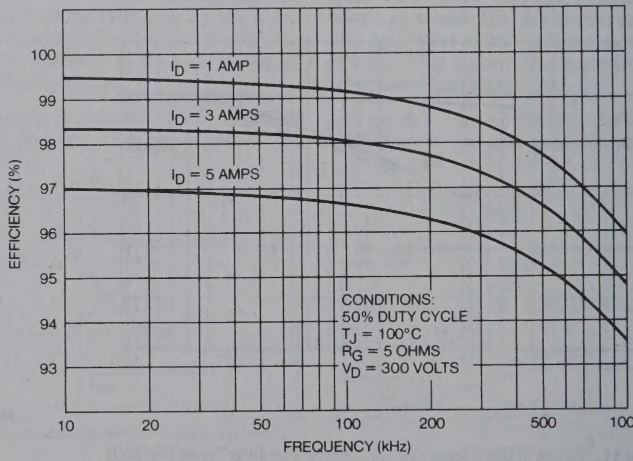


Figure 17. Switching Efficiency (IRF330)

"current crowding" in the base region, which causes hot spots. Because of the bipolar's negative temperature coefficient, these hot spots tend to further "hog" the current and cause instantaneous, catastrophic destruction of the die.

As any power transistor circuit designer will know, the rated maximum power dissipation of the bipolar actually applies only over a very limited range of collector voltage, typically up to 10% of rated V_{CEO}. At higher voltages, the dc power dissipation is severely limited by second breakdown. Typically, at rated voltage the permissible power dissipation is only 5% of full rated power.

The Safe Operating Area of the IRF330 series MOSFET is shown as an example in Figure 18. Note that the DC current is limited throughout the voltage range only by the 75 watt power dissipation slope. There are no secondary slopes in the DC dissipation curve (or the pulse curve) that indicate the second breakdown limit commonly seen on bipolar Safe Operating Area curves. Note also the high values of pulse current and the corresponding long time periods for which the pulse power can be safely tolerated.

The IRF330, for example, can tolerate 0.375 amperes at 200 volts on a DC basis. By contrast, the popular 2N6545, a bipolar transistor with the same voltage rating, but double the continuous current rating, has only a 0.06 ampere DC second breakdown limit at 200 volts. At one millisecond pulse width and 300 volts, the IRF330 rates at 1.0 amperes versus only 0.45 amperes for the 2N6545.

The absence of second breakdown means that the power MOSFET is generally a much more rugged device than the bipolar transistor. This is extremely important, both for "linear" and "switching" applications.

The V_{DS} absolute maximum rating of MOSFETs should not be exceeded by allowing them to operate in the avalanche region. However, it is possible to reliably turn off high level inductive currents, which can generate high voltage inductive transients, by using a simple voltage clamp circuit. All of IR's MOSFETs have a clamped inductive rating such that the maximum rated pulse current can be turned off with a 100 microhenry inductor in series. Because MOSFETs are very fast devices, caution must be taken that the voltage clamp device has a sufficiently fast response, and that it is closely coupled to the drain-source terminals. A zener diode connected physically as close as possible to the drain and source terminals generally will provide acceptable voltage clamping.

The transconductance, g_{fs}, of a MOSFET is maximum at the highest allowable drain currents. In contrast, the DC gain, h_{FE}, of a bipolar transistor, decreases drastically at high collector currents. The high transconductance of MOSFETs at high currents, combined with the excellent SOA rating, result in MOSFETs being superb pulse amplifiers. All of IR's power MOSFETs have a pulsed current rating, I_{DM}, that is at least twice the continuous current rating, I_D. IR's power MOSFETs operate excellently in the pulse region as long as the allowable average power dissipation, safe operating area, and ±20 volt maximum gate voltage ratings are not exceeded.

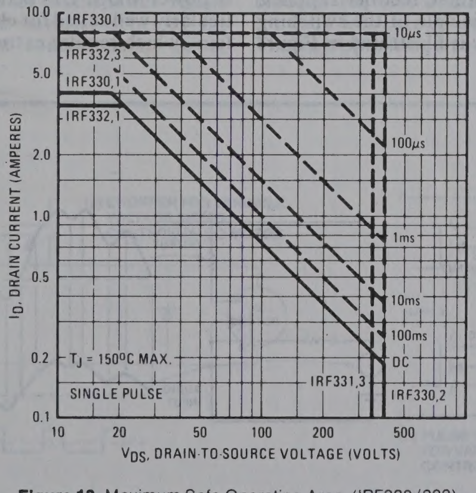


Figure 18. Maximum Safe Operating Area. (IRF330/333)

Temperature Stability

MOSFETs have outstanding gain and switching time stability with temperature variations, relative to the stability of typical bipolar transistors. The transconductance of IR Power MOSFETs typically varies less than ±20% from the 25°C value, over a −55°C to 125°C range. The DC current gain of a power bipolar commonly varies by a factor of 2 or 3 over this temperature range.

A rough comparison of the typical DC gain stability for an IR power MOSFET versus a power bipolar would yield a transconductance, g_{fs}, temperature coefficient of about −0.2% per °C versus a bipolar current gain, h_{FE}, temperature coefficient of about +0.8% per °C — a four-fold difference.

Reference to Figure 6 will show that the threshold voltage (bias point) and the transconductance (DC gain) move with temperature in compensating directions. Therefore, an operating point on the DC transfer characteristic maintains unusually good open loop stability. Drift-free operation becomes easy in a linear, closed loop system.

The switching time of IR power MOSFETs is essentially independent of operating temperature. This is a tremendous advantage relative to bipolar transistors, for which the 25°C switching times and associated power losses commonly increase by a factor of 2 or 3 at the higher actual operating temperatures. The extraordinary switching time stability of MOSFETs results because the response times are primarily dependent on the input capacitance, C_{iss}, which is essentially temperature invariant.

The on-resistance, $R_{D(ON)}$ of power MOSFETs, has a positive temperature coefficient, of approximately +0.7% per°C. This is an advantage in paralleling MOSFETs, and as has been seen it also accounts for their excellent safe operating area. However, in determining the on-state power losses in a switching mode, the increased value of $RD_{(ON)}$ at the actual maximum junction operating temperature must be used. Sufficient heatsink must always be used so that a thermal runaway situation cannot occur.

Paralleling

Power MOSFETs are easy to parallel, because the positive temperature coefficient forces current sharing among the paralleled devices. Current sharing resistors, with their associated power losses, are not necessary. Some resistance in series with the gates (typically 100 ohms) and close paralleled lead connections may be necessary to assure that the good high frequency response of the MOSFETs does not cause oscillations.

MOS Caution

The ±20 volt absolute maximum gate voltage rating of IR power MOSFETs should never be exceeded, or permanent damage can occur.

Zener diode protection should be used if there is a danger of transient gate overvoltages. This caution applies also to the buildup of static charge. IR power MOSFETs have large gate capacitances and thick oxide layers relative to low level MOS devices, where static charge damage can be particularly dangerous. Though significantly more rugged than such low level MOS devices, reasonable precautions which are normally taken in handling MOS devices should be observed until the installation of MOSFETs in a circuit.

APPLICATIONS

Power MOSFETs offer tremendous operating advantages over conventional bipolar transistors, and they will undoubtedly replace bipolars in many existing applications. In order to take full advantage of their unique operating features, and thus to produce an optimum overall system design, it will almost never be sufficient merely to make a one-for-one replacement of a bipolar with a MOSFET in an otherwise unmodified circuit. The much lower drive requirement of the MOSFET will usually mean that very significant simplifications can be made in the drive circuitry; the vastly superior switching speed will offer the possibility for lower losses, or higher operating frequency, or both; and the superior safe operating area will offer greater loading and overloading capability, and minimization or elimination of protective snubber components.

Many potential applications of Power MOSFETs are obvious, and are already being actively pursued by circuit development engineers throughout the world. A great number of as yet unexplored applications will surely emerge, as the unique advantages of IR's power MOSFETs become more widely understood, and as power MOSFET technology itself develops and matures.

In the following sections we will briefly review some of the most obvious application areas. This may help to stimulate the imagination of the reader to perceive new applications for power MOSFETs in his own particular field of expertise.

Switching Power Supplies

Switching DC power supplies are rapidly replacing conventional 50 or 60Hz transformer/rectifier supplies. The basic principle of the switching power supply is illustrated in Figure 19. This switching scheme by comparison with the conventional line frequency power supply, offers smaller overall size, due to much smaller transformer and smoothing components, faster response, better regulation, and higher efficiency.

Switching power supplies presently use bipolar transistors, and usually operate in the 20-35 kHz frequency range. Higher operating frequencies are not generally practical, because bipolar switching times are too long. From the system viewpoint, an increase in the switching frequency to 200 kHz or higher would offer the possibility for further reductions in size, weight, and response time. Such high operating frequencies now become a practical reality, with the availability of IR's power MOSFETs. Other potential advantages would be elimination of electrolytic capacitors, smaller EMI filters, and simplified drive and snubber circuits.

The MOSFET also offers advantages in the existing 20 to 30 kHz range, in terms both of reduced overall losses, because of reduced switching losses, and reduced circuit complexity, because of the minimal gate drive requirement.

Audio Amplifiers

The power MOSFET offers a quite linear input to output transfer characteristic. This means that with appropriate biasing it can be used as a simple high quality audio amplifier, illustrated in a simplified form in Figure 20.

The excellent Safe Operating Area of power MOSFETs make them particularly well suited for class B amplifiers, which require extreme low fre-

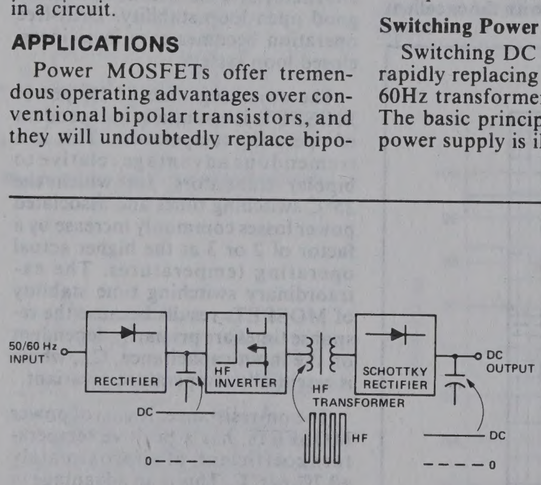


Figure 19. Basic Principle of Switching Power Supply

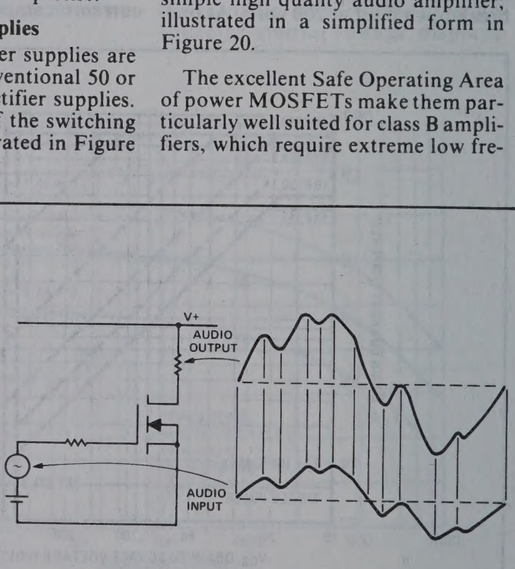


Figure 20. Basic Principle of Audio Amplification using Power MOSFET

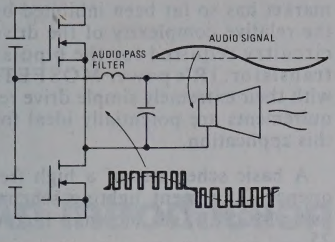


Figure 21. Class D Audio Amplifier — Basic Principle

quency response at high power levels. The wide MOSFET bandwidth makes good high frequency response of the amplifier easy.

Another type of audio amplifier uses the class D pulsewidth modulation principle, illustrated diagrammatically in Figure 21. Implementation of this type of amplifier with bipolar transistors has not generally been successful, because the carrier frequency must be much higher than the audio frequency to produce a good quality output. The relatively long switching times of the bipolar are a fundamental limitation. With the availability of IR's power MOSFETs, these limitations are eliminated. This type of approach offers the possibility for an audio amplifier of extremely high efficiency, small size, and high fidelity.

Motor Speed Control

The use of bipolar transistors for speed control of both DC and AC motors is taking a firm hold in the marketplace, for power ratings up to several tens of horsepower. Basic chopper and inverter schemes for motor speed control using power MOSFETs are shown in Figure 22. The use of variable frequency DC to AC inverters, for efficient control of the speed of AC induction motors is becoming particularly topical in view of the present day emphasis on energy saving techniques.

In these circuits the switching frequency typically will be in the range of a few hundred Hz, to a few kHz. This, of course, is well within the capability of bipolar transistors. MOSFETs can however offer significant advantages, because of their substantially reduced drive power requirements, and improved safe operating area and ruggedness. These features will result in simplification of peripheral circuitry, improved reliability, and improved response time.

The ease of paralleling power MOSFETs for higher power output is also an important advantage, whilst the somewhat higher conduction voltage drop and hence higher power loss of the MOSFET is but a slight disadvantage — more theoretical than practical. The extra heatsink required to accommodate the greater power dissipation of the MOSFET is minimal indeed, and is greatly outweighed by the advantages to be gained.

AM Transmitters

Conventional AM broadcasting transmitters operate in the 0.5 to 1.6 MHz range. They use vacuum tubes, which are relatively bulky and unreliable. Newer designs are using parallel connected bipolar transistors.

Typically an AM transmitter using bipolars requires about 60 devices, for each kilowatt of output power. The high operating frequency pushes the limits of bipolar operation, paralleling is difficult, and the required reliability is not easy to achieve.

Power MOSFETs are capable of operation within the required frequency range, and are easily parallelable. The total number of devices would be drastically reduced; for example 8 IRF350's would be needed for each kilowatt of output power, as compared to 60 bipolar transistors. Another advantage of the MOSFET system would be that it is able to handle mismatch and fault conditions, and the driver stages would be much simpler. A basic schematic of an AM transmitter using power MOSFETs is shown in Figure 23.

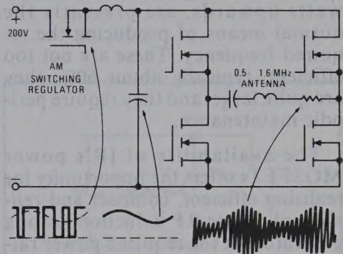
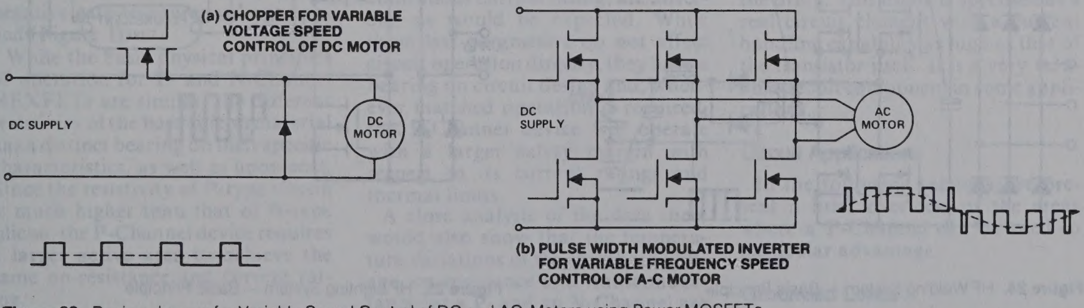


Figure 23. AM Transmitter — Basic Principle

Induction Heating

The heating of metal by energizing an induction coil that couples magnetic flux and induces a flow of eddy current into the work piece is an established principle, that is widely used throughout industry. It is an efficient, clean and cost effective means of melting, heating, hardening, annealing and welding of metals.



(a) CHOPPER FOR VARIABLE VOLTAGE SPEED CONTROL OF DC MOTOR

(b) PULSE WIDTH MODULATED INVERTER FOR VARIABLE FREQUENCY SPEED CONTROL OF A-C MOTOR

Figure 22. Basic schemes for Variable Speed Control of DC and AC Motors using Power MOSFETs

Induction heating systems cover a wide range of frequencies, starting at line frequency and progressing up to around 500kHz. The lower frequency ranges, up to 20kHz or so, today are generally covered by variable frequency thyristor inverters, which have now largely replaced the older fixed frequency rotating generator sets.

Power levels of induction heating equipment extend up to several megawatts at the lower end of the frequency spectrum. As the required frequency increases, generally the power requirement decreases.

For frequencies in the 100 to 500kHz range vacuum tube oscillators, with ratings from a few kilowatts upwards, are presently the normal means of producing the required frequency. These are not too efficient, typically about 60%, they are quite large, and they require periodic maintenance.

The availability of IR's power MOSFETs offers the opportunity for realising efficient, compact and reliable solid state RF induction heating generators at the required power ratings, at frequencies up to 500kHz.

Another use of induction heating that has been proposed is in domestic cooking. Heating currents are induced from an induction coil directly into the cooking utensil. This technique offers dramatic improvements in efficiency and response time.

Commercial exploitation of this principle has not so far generally been successful, primarily because of the complexity of the required high frequency inverter circuitry. The availability of IR's power MOSFETs makes possible a complete reappraisal of the induction cooker.

High Frequency Welding

Modern DC power supplies use high frequency switching techniques to obtain greater compactness, improved efficiency and faster response. This very same switching technique is also applicable to DC welding supplies. These traditionally use a bulky mains frequency transformer, often a ballast impedance to obtain the required output regulation, and an output rectifier to provide the required DC.

Figure 24 shows a basic schematic of a possible high frequency welding system using power MOSFETs. IR's power MOSFETs can deliver several kilowatts of power at frequencies well above the audio range; this type of scheme would provide a compact, portable, silent, efficient welder, with fast response and excellent controllability.

Fluorescent Lighting

Conventional mains frequency fluorescent lighting requires bulky inductive ballasting and power factor capacitors, and is relatively inefficient. It is well known that by using high frequency to supply the fluorescent tube, power consumption for a given light output can be reduced by 30 to 35%, whilst tube life can be substantially increased, and bulky ballast components are eliminated.

- Fluorescent lighting schemes using high frequency bipolar transistor inverters are presently used in applications such as transportation and emergency lighting systems.

Application of high frequency techniques to the general consumer market has so far been inhibited by the relative complexity of the drive circuitry required for the bipolar transistor. IR's power MOSFETs with their extremely simple drive requirements are potentially ideal for this application.

A basic schematic of a high frequency fluorescent lighting scheme using MOSFETs is shown in Figure 25.

Other Applications

The applications discussed above are just a few of the many potential uses of IR's power MOSFETs. Other immediate application areas are high frequency generators for diathermy, drivers for high power bipolar transistors and thyristors, pulsewidth modulated high current supplies for spark erosion, beam control of video displays for computer terminals, and VLF and HF generators.

Summary

Power MOSFETs have numerous operating characteristics which are distinctly superior to those of power bipolar transistors. These superiorities occur because MOSFETs have fundamentally different operating principles. Understanding the operating principles and superiorities of MOSFETs will allow the creative designer to make fundamental improvements in many types of transistorized products, as well as to innovate entirely new types of product.

The introduction of IR HEXFETs — the world's most advanced form of power MOSFETs — further underscores the importance of MOSFET technology for the circuit designs of the future. □

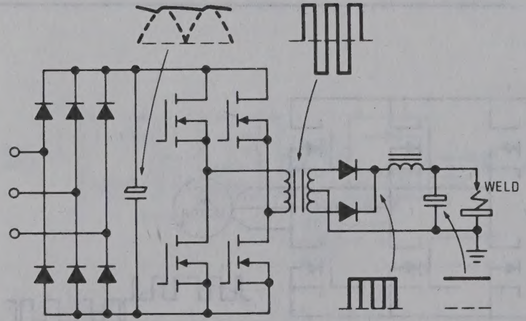


Figure 24. HF Welding System — Basic Principle

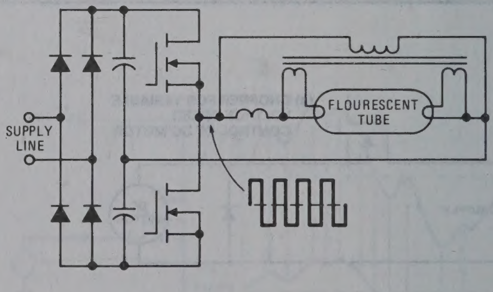


Figure 25. HF Lighting System — Basic Principle

CHAPTER 3

APPLICATION NOTE 940

An Introduction to International Rectifier P-Channel HEXFETs™

By **S. CLEMENTE,** Senior Applications Engineer, International Rectifier

With the introduction of International Rectifier's line of P-Channel power HEXFETs, a new option is available to the designer that can simplify circuitry while optimizing performance and parts count. This application note discusses the basic characteristics of P-Channel HEXFETs and gives a conceptual overview of typical circuit applications.

Basic Characteristics of P-Channel HEXFETs

Like their N-Channel counterparts, International Rectifier P-Channel HEXFETs are all presently enhancement mode devices; that is, application of voltage between the gate and the source terminals enhances the conductivity and allows current to flow, while no drain current flows when the gate is shorted to the source. For drain current to flow, the gate voltage has to be increased (in absolute value) towards the drain voltage. In a P-Channel device, the conventional flow of drain current is in the "negative" direction — that is, current flows out of the drain, with a negative gate-to-source voltage applied (Figure 1).

While the basic physical principles of operation for P- and N-Channel HEXFETs are similar, the different resistivity of the base silicon material has a distinct bearing on their specific characteristics, as well as upon cost. Since the resistivity of P-type silicon is much higher than that of N-type silicon, the P-Channel device requires a larger active area to achieve the same on-resistance and current rating.

This difference in resistivity of the basic silicon material is an obstacle to the construction of a P-Channel device that is truly electrically complementary in all respects to an N-Channel counterpart. Since for a given drain-source voltage capability, the on-resistance is the most basic parameter, the P-Channel HEXFET device will have the larger active area needed to achieve the same on-resistance as its complementary N-Channel counterpart. Gate threshold voltage, transconductance and self-capacitances are equalized as nearly as possible by accurate device design. Table 1 shows the parameters of two typical complementary P- and N-Channel HEXFETs (the IRF9130 and the IRF120) and shows to what extent their major parameters match one another. Voltage ratings, on-resistance, threshold voltage and, of course, package configuration, are exactly the same. Input capacitance and transconductance are also fairly closely matched. However, those parameters that are closely related to the die area, specifically thermal resistance, pulsed current rating, safe operating area and, to some extent, continuous current rating, are different, as would be expected. While these last parameters do not affect circuit operation directly, they have a bearing on circuit design and, whenever matched operation is required, the P-Channel device will operate with a larger safety margin with respect to its current ratings and thermal limits.

A close analysis of the data sheet would also show that the temperature variations of the threshold voltage, on-resistance and transconductance for a P- and an N-Channel are slightly different. This difference can, however, be considered a second order effect in most practical applications.

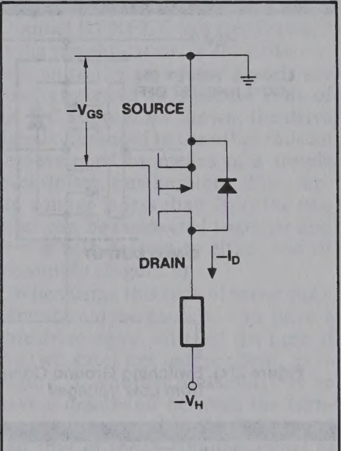


Figure 1. P-Channel power HEXFET

As shown in Figure 1, the P-Channel HEXFET, like its N-Channel counterpart, has an integral reverse rectifier, whose anode is connected to the drain. This diode is specified as a real circuit element with a current handling capability as high as that of the transistor itself. It is a very valuable circuit component in some applications.

Circuit Applications

In the following sections, we present a brief overview of the areas where a P-Channel can be used to particular advantage.

Grounded Loads

One area where P-Channel HEXFETs yield circuit simplification and cost savings is where the load is connected to ground. This is mandated in many automotive and aircraft applications and, sometimes, in household appliances. In these applications, in addition to wide safe operating area and excellent switching characteristics that are common to all HEXFETs, the use of a P-Channel device allows the load to be tied to the drain so that the gate drive can be referenced to one side of the supply. If an N-Channel were used, a separate supply would be required, referenced to the source, for the gate drive voltage.

Figure 2(a) shows how such a circuit would operate when driven from a C-MOS gate. However, if the load is operated at voltages above 15V, the logic ground cannot be connected to the load ground, and a separate supply is needed for the logic circuits,

Table 1.

	N-Channel	P-Channel
Device Type	IRF120	IRF9130
Drain-to-Source Voltage (Max.)	100V	-100V
Die Size	$8.04mm^2$	$13.25mm^2$
On-Resistance (Maximum)	0.3Ω	0.3Ω
On-State Drain Current @ $T_C = 90°C$	6A	-8A
Pulsed Drain Current	15A	-30A
Gate Threshold Voltage (Minimum-Maximum)	2 to 4V	-2 to -4V
Forward Transconductance (Typical)	2.5 S	3.5 S
Input Capacitance (Typical)	450pF	500pF
Output Capacitance (Typical)	200pF	300pF
Reverse Transfer Capacitance (Typical)	50pF	100pF
Maximum Thermal Resistance	3.12 deg. C/W	1.67 deg. C/W
Package	TO-3	TO-3

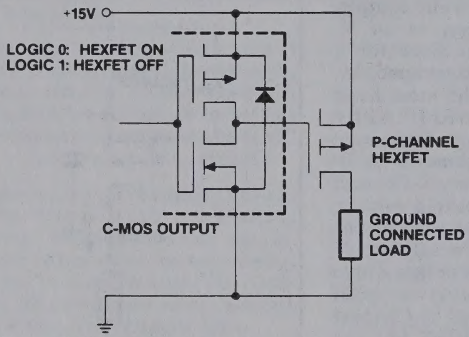


Figure 2(a). Switching Ground Connected Loads Operating from Low Voltages

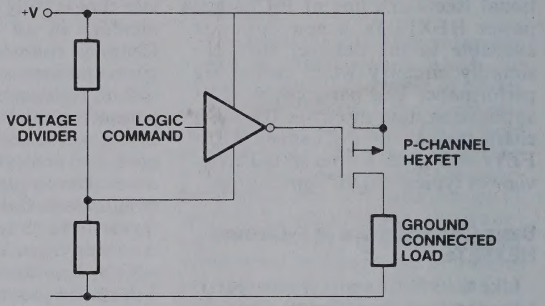


Figure 2(b). Switching Ground Connected Load at Higher Voltages

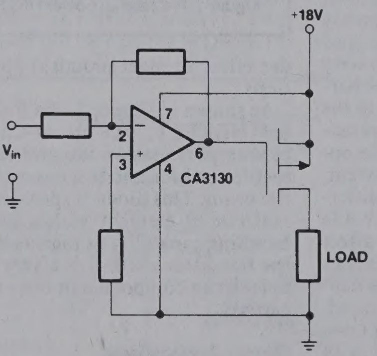


Figure 3(a). Driving Grounded Load in Linear Mode (Low Voltage)

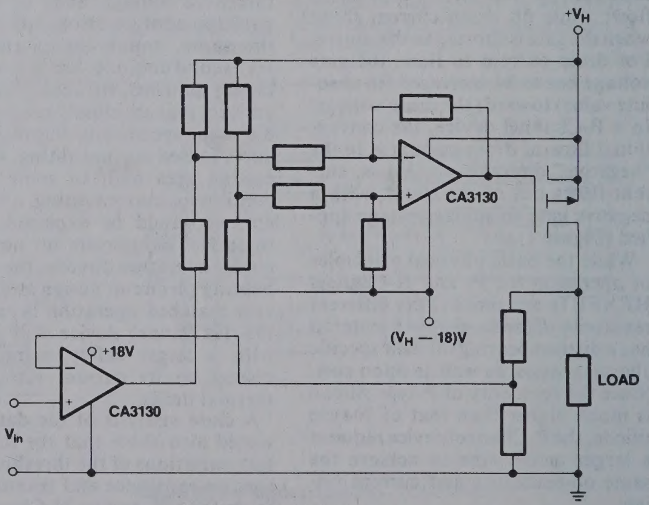


Figure 3(b). Driving Grounded Load in Linear Mode (High Voltage) as shown in Figure 2(b). An alternative approach is to drive the P-Channel HEXFET through a level shifter, as shown in Figure 5. Notice that to achieve the same result with an N-Channel HEXFET, a separate supply referenced to the source would be required.

A P-Channel device can also be operated in linear mode as shown in Figure 3. The device lends itself readily to voltage or current regulation which can be achieved through the use of suitable feedback. In the applications shown in Figures 3(a) and 3(b), the device drops whatever excess voltage is available from the unregulated supply. For parallel connection of devices, or where fast slew rate is important, a current boosting stage at the output of the operational amplifier may be required.

Totem Pole Switching Circuits

One of the most common building blocks for switching applications is the "totem pole." It is used in a variety of applications, such as switching power supplies, DC-to-AC converters, AC motor speed controllers, AM transmitters and Class D switching audio amplifiers.

Figure 4 shows one such circuit, implemented with two N-Channel HEXFETs, and its associated gate drive circuit. Since the drive circuits have to be referenced to the respective sources, they are isolated from each other. The most commonly used techniques to develop an "isolated" gate drive signal are optical isolators, transformer coupling and "bootstrapping." Optical isolators, shown in Figure 4, require a separate supply and are relatively slow and susceptible to noise. Pulse transformers, on the other hand, can only transfer to the secondary an AC signal (Figure 8), and hence have a limitation on the maximum and minimum possible switching duty cycle. They also always have some unwanted amount of leakage inductance. "Bootstrapping" is a technique for deriving a local gate drive voltage via a capacitor connected in the main drain circuit. Whereas it is satisfactory in many applications, it again has limitations regarding permissible duty cycle and maximum operating frequency.

The totem pole shown in Figure 5, using one N-Channel and one P-Channel HEXFET, is a step forward in the simplification of the drive circuit, since the gate drive signals are now referenced to separate ends of the DC supply. As shown, the drive signal referenced to the other rail can be developed by means of a simple level shifter. Furthermore, if the supply voltage is less than 20V, the two gates can be connected together and driven with respect to either end of the supply (Figure 6).

When using this type of totem pole, care should be exercised to have a gate drive signal with fast rise time. If the two gates are independent, as in Figure 5, another possibility is to have a deadband between the turn-on gate command of the P-Channel and that of the N-Channel equal to the rise time of the gate drive signal. Unless this is done, a short circuit current will flow through the two devices during the transition times,

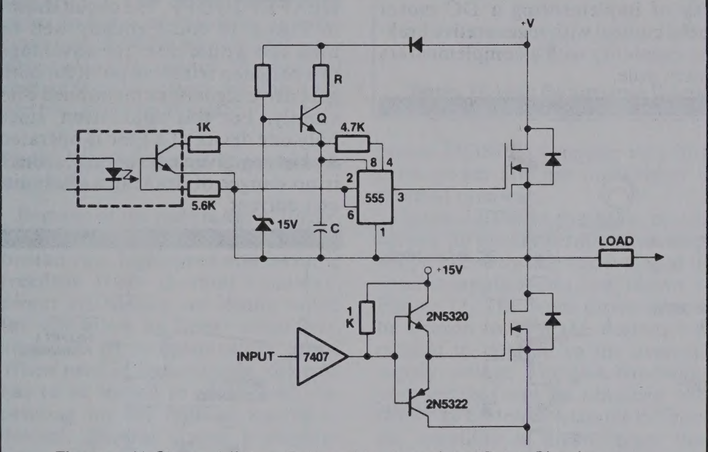


Figure 4. N-Channel Totem Pole and its Associated Drive Circuits

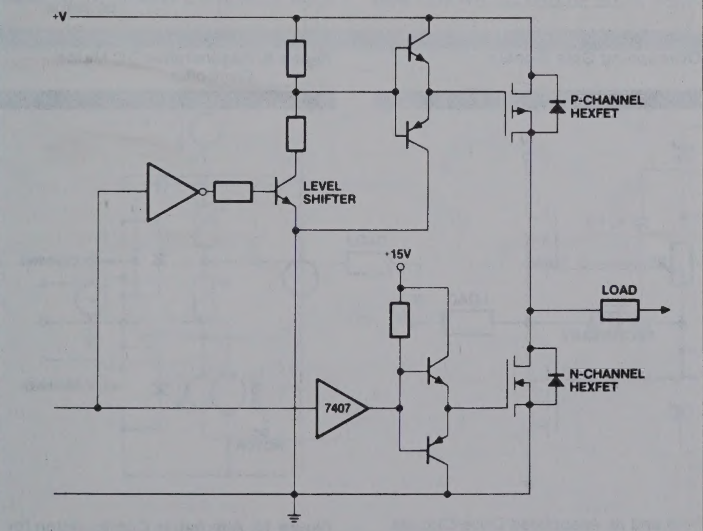


Figure 5. P/N-Channel Combination Totem Pole and its Associated Drive Circuits. Load is Connected to the Drains.

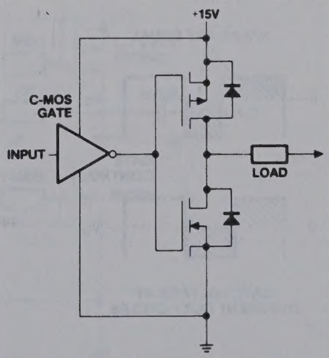


Figure 6. P/N-Channel HEXFET Totem Pole with Drive Circuit for Operation at Low Voltages

as shown in Figure 7. However, the current regulating characteristic of power MOSFETs tends to limit the amount of this current and, while it may significantly increase the switching losses, it would not necessarily reach catastrophic values.

Should a common reference be desired for both gate drive signals, the circuit configuration shown in Figure 8 can be used. The positions of the P- and N-Channel HEXFET devices have been interchanged so that both have the load connected to the source. The gate drive signals are now referenced to the same point; however, this point is neither of the two supply leads. This is probably the circuit configuration that affords the simplest and most noise-immune gate drive circuit. An added advantage of this circuit is that it will not draw a short circuit current (Figure 7), because it is inherently impossible to drive both devices ON simultaneously.

Application of the Switching Totem Pole

The switching totem pole is used in a number of different applications. Some of the most common are the following:

- DC-to-AC inverters for battery operated supplies, stand-by and uninterruptible power systems.
- Variable frequency inverter for high efficiency speed control of AC induction motors.
- Regenerative speed control of DC motors.

Taking as an example this last application, we show in Figure 9 a way of implementing a DC motor speed control with regenerative braking capability with a complementary totem pole.

In the "motoring" mode of operation, HEXFET 1 is switched ON and OFF, at an appropriate repetition rate, and provides control of the average voltage applied to the motor. HEXFET 2 is OFF, but its integral reverse body-drain diode acts as the conventional freewheeling rectifier, and carries the freewheeling motor current during the periods when HEXFET 1 is OFF. When the motor is required to act as a generator and return energy to the DC source, HEXFET 2 is chopped ON and OFF, and controls the current fed back from the motor to the supply. In this operating mode, HEXFET 1 is OFF, but its integral reverse rectifier carries motor current back to the DC source during the intervals when HEXFET 2 is OFF. The circuit shown in Figure 10 could equally well be used and would offer the advantage of a common reference point for both gate drive signals, as mentioned previously. For this application, since only one device at a time is operated within any given control cycle, there is no danger of drawing a short circuit current.

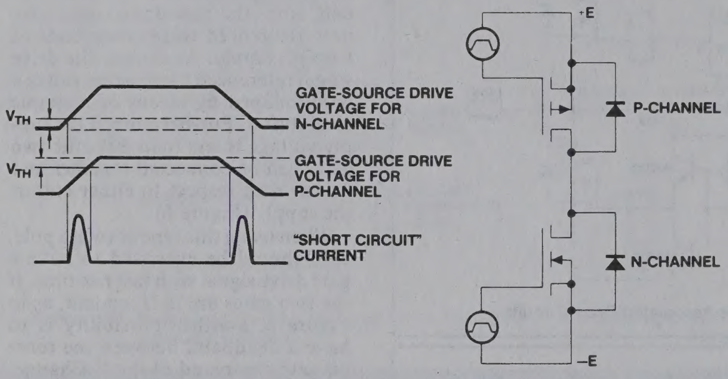

+E
V_{TH}
GATE-SOURCE DRIVE VOLTAGE FOR N-CHANNEL
V_{TH}
GATE-SOURCE DRIVE VOLTAGE FOR P-CHANNEL
"SHORT CIRCUIT" CURRENT
P-CHANNEL
N-CHANNEL
–E

Figure 7. Short Circuit Current Caused by Overlapping Gate Signals

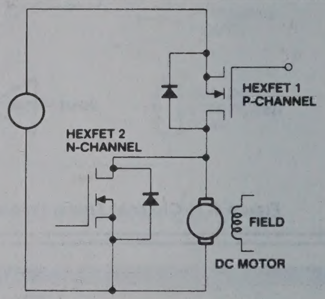


Figure 9. Regenerative DC Motor Controller

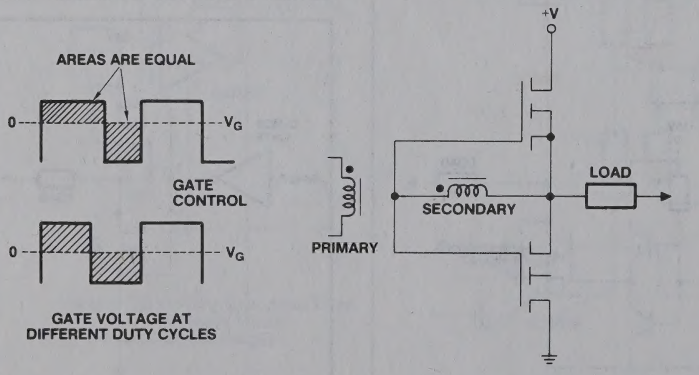


Figure 8. N/P-Channel Combination Totem Pole and its Associated Drive Circuits

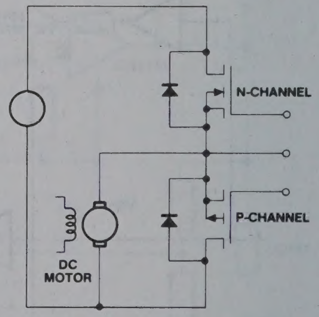


Figure 10. Alternative Configuration for the Regenerative DC Motor Controller

Another consideration in choosing between the circuit connections of Figure 9 or Figure 10 is the current rating of the two devices. Normally, the device that is being switched during regeneration does not need to have a current rating as high as the motoring device, since friction and windage in the motor contribute to the braking torque. Therefore, the P-Channel HEXFET, because of its lower current rating for a given die size, may be a better choice for the regenerative operation.

Apart from being the basic building block of a large variety of inverter circuits, totem poles can be profitably used to drive large transistors or a parallel combination of them whenever high performance is required (Figure 11). This circuit can be used either in linear or switching applications and provides a good low impedance gate drive source. The integral reverse rectifiers clamp possible voltage transients on the gate.

Linear Application of Complementary Pairs

Because of the wide range of linearity of g_{fs}, immunity from secondary breakdown, high speed and intrinsic freedom from thermal runaway, power HEXFETs are ideally suited for operation as linear amplifiers, alone or in complementary pairs. When used in linear mode, the gate has to be biased to some level, depending on the type of operation desired. Several circuit configurations will achieve this end; they are inevitably simpler than would be required for bipolar transistors, since power MOSFETs require very little drive power and are not subject to thermal runaway.

Figure 12 shows the basic biasing scheme for linear operation, but much simpler versions can be developed for specific applications, as shown in Figure 13. The zener diodes should be chosen to give the desired bias current in relation to the available supply voltage. The gain bandwidth product that can be obtained with this stage driven by a simple differential amplifier is much larger than what can be obtained by a more complex bipolar configuration. The slew rate would also be much better.

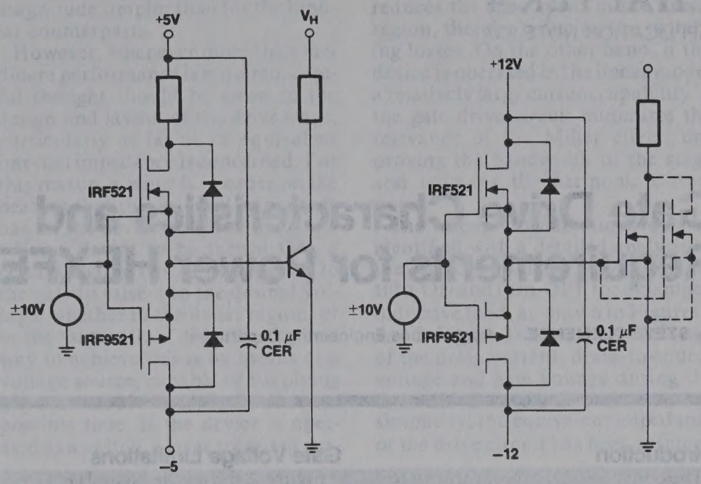


Figure 11. High Performance Drivers

Summary

P-Channel HEXFETs are electrical complements to International Rectifier N-Channel types. The availability of these devices offers new design options to the circuit engineer, and opens up the possibility for new HEXFET applications that were not before feasible with N-Channel types alone. ☐

Acknowledgements

The amplifier circuit shown in Figure 13 was developed by H. Schar of International Rectifier GmbH, Frankfurt, West Germany.

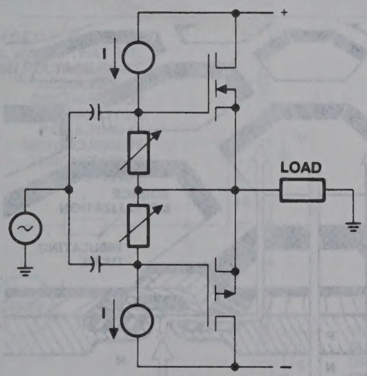


Figure 12. Basic Biasing Scheme for Linear Operation

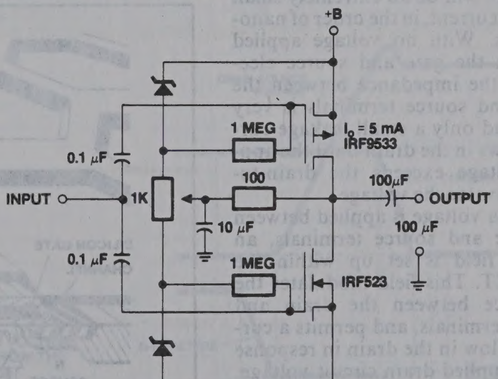


Figure 13. Simple Biasing Scheme for linear Operation

CHAPTER 4

APPLICATION NOTE 937

Gate Drive Characteristics and Requirements for Power HEXFETs™

By STEVE CLEMENTE, Applications Engineering Department

Introduction

The conventional bipolar transistor is essentially a current-driven device. As illustrated in Figure 1(a), a current must be applied between the base and emitter terminals to produce a flow of current in the collector. The amount of a drive required to produce a given output depends upon the gain, but invariably a current must be made to flow into the base terminal to produce a flow of current in the collector.

The HEXFET is fundamentally different; it is a voltage-controlled power MOSFET device. A voltage must be applied between the gate and source terminals to produce a flow of current in the drain (see Figure 1b). The gate is isolated electrically from the source by a layer of silicon oxide. Theoretically, therefore, no current flows into the gate when a DC voltage is applied to it — though in practice there will be an extremely small leakage current, in the order of nanoamperes. With no voltage applied between the gate and source electrodes, the impedance between the drain and source terminals is very high, and only a small leakage current flows in the drain until the applied voltage exceeds the drain-to-source avalanche voltage.

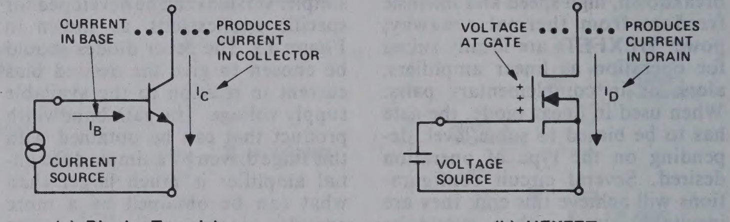
When a voltage is applied between the gate and source terminals, an electric field is set up within the HEXFET. This field modulates the resistance between the drain and source terminals, and permits a current to flow in the drain in response to the applied drain circuit voltage.

Although it is common knowledge that HEXFET transistors are more easily driven than bipolars, a few basic considerations have to be kept in mind in order to avoid a loss in performance or outright device failure.

Gate Voltage Limitations

Figure 2 shows the basic HEXFET structure. The silicon oxide layer between the gate and the source regions can be easily perforated if the gate-to-source voltage exceeds 20V, even if the current is limited to a very low value.

Since the perforation of this oxide layer is one of the most common causes of device failure, great care should be exercised not to exceed the gate-to-source maximum voltage rating. It should be kept in mind, also, that even if the applied gate voltage is kept below the maximum rated gate



(a) Bipolar Transistor **(b) HEXFET**

Figure 1. Bipolar Transistor is Current Driven, HEXFET is Voltage Driven

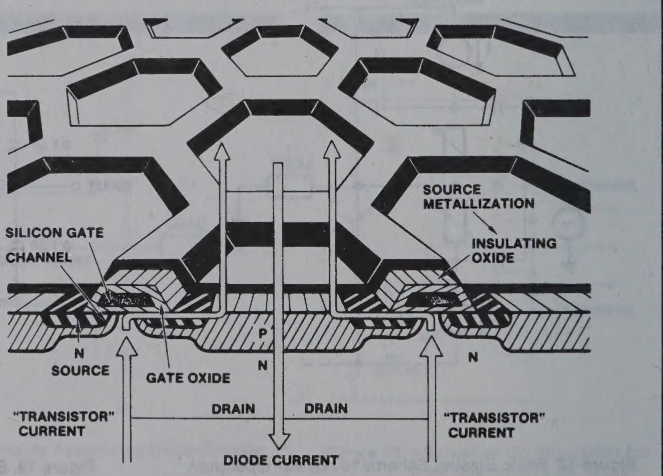


Figure 2. Basic HEXFET Structure

voltage, the stray inductance of the gate connection, coupled with the gate capacitance, may generate ringing voltages that could lead to the destruction of the oxide layer. Overvoltages can also be coupled through the drain-gate self-capacitance due to transients in the drain circuit. For these reasons, it is advisable to connect a zener diode between gate and source to provide a reliable clamp on the gate voltage. A small resistor or a ferrite bead will normally be adequate to swamp out undesired oscillations.

The Impedance of the Gate Circuit

In comparing power HEXFETs to bipolar transistors, the point is often made that the former require hardly any drive power. This is certainly true, and is the main reason why the drive circuit is normally an order of magnitude simpler than for the bipolar counterparts.

However, whenever more than mediocre performance is required, careful thought should be given to the design and layout of the drive stage, particularly as far as its equivalent internal impedance is concerned. For this reason, a word is in order on the bearing that this internal impedance has on the device performance.

For a device to be turned ON, a certain charge has to be supplied to the gate to raise it to the desired voltage, whether in the linear region, or in the "saturation". Ideally, the best way to achieve this is by means of a voltage source, capable of supplying any amount of current in the shortest possible time. If the device is operated as a switch, a large transient current capability of the drive circuit reduces the time spent in the linear region, thereby reducing the switching losses. On the other hand, if the device is operated in the linear mode, a relatively large current capability in the gate drive circuit minimizes the relevance of the Miller effect, improving the bandwidth of the stage and reducing the harmonic distortion.

The above considerations can be identified with a detailed analysis of the basic switching waveforms at turn-ON and turn-OFF for a clamped inductive load, as shown in Figures 3 and 5. Figure 3 shows the waveforms of the drain current, drain-to-source voltage and gate voltage during the turn-ON interval. For the sake of simplicity, the equivalent impedance of the drive circuit has been assumed

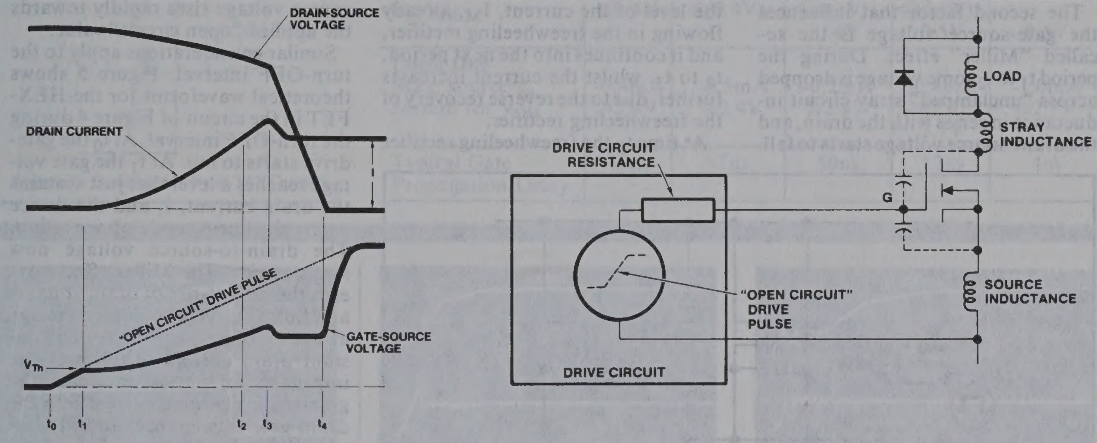
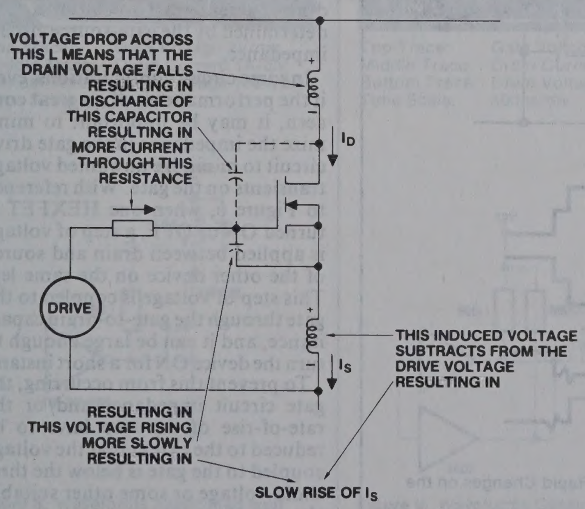


Figure 3. Waveforms at Turn-On



VOLTAGE DROP ACROSS THIS L MEANS THAT THE DRAIN VOLTAGE FALLS RESULTING IN DISCHARGE OF THIS CAPACITOR RESULTING IN MORE CURRENT THROUGH THIS RESISTANCE
+
−
I_D
DRIVE
+
−
I_S
THIS INDUCED VOLTAGE SUBTRACTS FROM THE DRIVE VOLTAGE RESULTING IN
RESULTING IN THIS VOLTAGE RISING MORE SLOWLY RESULTING IN
SLOW RISE OF I_S

Figure 4. Diagrammatic Representation of Effects When Switching-ON

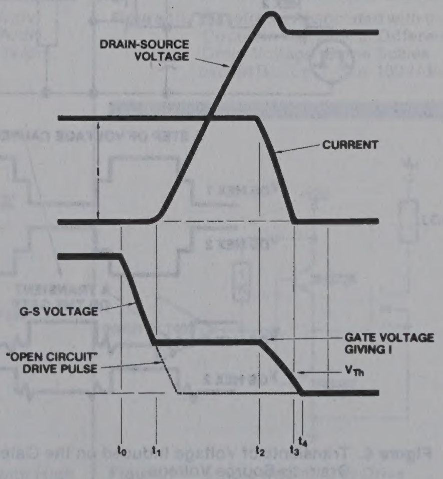


Figure 5. Waveforms at Turn-OFF

as purely resistive.

At time, t_0, the drive pulse starts to rise. At t_1 it reaches the threshold voltage of the HEXFET, and the drain current starts to increase. At this point, two things happen which make the gate-source voltage waveform deviate from its original "path". First, inductance in series with the source which is common to the gate circuit develops an induced voltage, as a result of the increasing source current. This voltage counteracts the applied gate drive voltage, and slows down the rate of rise of voltage appearing directly across the gate and source terminals; this in turn slows down the rate of rise of the source current. This is a negative feedback effect; increasing current in the source produces a counteractive voltage at the gate, which tends to resist the change of current.

The second factor that influences the gate-source voltage is the so-called "Miller" effect. During the period t_1 to t_2 some voltage is dropped across "unclamped" stray circuit inductance in series with the drain, and the drain-source voltage starts to fall. The decreasing drain-source voltage is reflected across the drain-gate capacitance, pulling a discharge current through it, and increasing the effective capacitive load on the drive circuit. This in turn increases the voltage drop across the source impedance of the drive circuit, and decreases the rate of rise of voltage appearing between the gate and source terminals. Obviously, the lower the impedance of the gate drive circuit, the less this effect will be. This also is a negative feedback effect; increasing current in the drain results in a fall of drain-to-source voltage, which in turn slows down the rise of gate-source voltage, and tends to resist the increase of drain current. These effects are illustrated diagramatically in Figure 4.

This state of affairs continues throughout the period t_1 to t_2, whilst the current in the HEXFET rises to the level of the current, I_M, already flowing in the freewheeling rectifier, and it continues into the next period, t_2 to t_3, whilst the current increases further, due to the reverse recovery of the freewheeling rectifier.

At time t_3 the freewheeling rectifier starts to support voltage, whilst the drain current and the drain voltage start to fall. The rate of fall of drain voltage is now governed almost exclusively by the Miller effect, and an equilibrium condition is reached, under which the drain voltage falls at just the rate necessary for the voltage between gate and source terminals to satisfy the level of drain current established by the load. This is why the gate-to-source voltage falls as the recovery current of the freewheeling rectifier falls, then stays constant at a level corresponding to the drain current, whilst the drain voltage is falling. Obviously, the lower the impedance of the gate-drive circuit, the higher the discharge current through the drain-gate self-capacitance, and the faster will be the full time of the drain voltage.

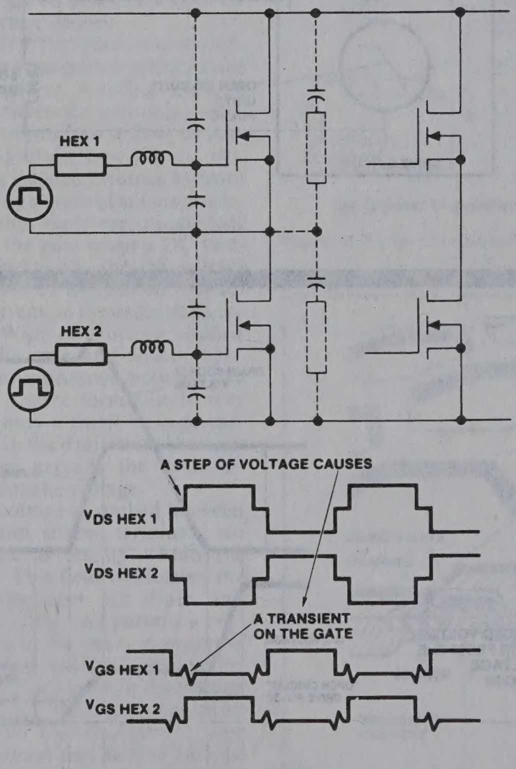


Figure 6. Transients of Voltage Induced on the Gate by Rapid Changes on the Drain-to-Source Voltage

Finally, at time t_4, the HEXFET is switched fully ON, and the gate-to-source voltage rises rapidly towards the applied "open circuit" value.

Similar considerations apply to the turn-OFF interval. Figure 5 shows theoretical waveforms for the HEXFET in the circuit of Figure 4 during the turn-OFF interval. At t_0 the gate-drive starts to fall. At t_1 the gate voltage reaches a level that just sustains the drain current, I, and the device enters the linear mode of operation. The drain-to-source voltage now starts to rise. The Miller effect governs the rate-of-rise of drain voltage, and holds the gate-to-source voltage at a level corresponding to the constant drain current. The lower the impedance of the drive circuit, the greater the charging current into the drain-gate capacitance, and the faster will be the rise time of the drain voltage. At t_3 the rise of drain voltage is complete, and the gate voltage and drain current start to fall at a rate determined by the gate-source circuit impedance.

In some circuit configurations, even if the performance is of no great concern, it may be important to minimize the impedance in the gate drive circuit to minimize unwanted voltage transients on the gate. With reference to Figure 6, when one HEXFET is turned ON or OFF, a step of voltage is applied between drain and source of the other device on the same leg. This step of voltage is coupled to the gate through the gate-to-drain capacitance, and it can be large enough to turn the device ON for a short instant.

To prevent this from occurring, the gate circuit impedance and/or the rate-of-rise of the step have to be reduced to the extent that the voltage coupled to the gate is below the threshold voltage or some other suitably chosen safe value.

Driving HEXFETs From TTL

Table 1 shows the guaranteed sourcing and sinking currents for different TTL families at their respective voltages. From this table, taking as an example the 74LS series, it is apparent that, even with a sourcing current as low as 0.4 mA, the guaranteed logic one voltage is 2.4V (2.7 for 74LS and 74S), and that is lower than the possible threshold of a HEXFET. The use of a pull-up resistor on the output (Figure 7) would take this voltage up to 5V, but it would still not be sufficient to guarantee "saturated" switching of the HEXFET, unless the current to be switched is substantially less than the rated value of the HEXFET.

More specifically, with reference to the output characteristics (Figure 3 of the data sheet), it can be seen that for a low voltage device (e.g., IRF130) the drain current corresponding to a gate voltage of 5V is approximately half its DC rated value, while for a high voltage device (e.g., IRF330) it is higher than the DC rated current. It should be emphasized though, that the curves show typical values and that, with a $V_{GS} = 5V$, saturation is not guaranteed for either DC or pulse rated conditions for any device.

Figure 8 shows a typical application of a TTL inverter driving a IRF320 with the waveforms that would normally be expected. The 74LS05 is an open collector device, but waveforms do not change significantly for a totem pole device. With reference to the drain voltage (bottom waveform) it is apparent that the device turns on much more slowly than it turns off. This is because the gate-to-source and gate-to-drain capacitances are charged exponentially through the pull-up resistor, while they are discharged through a saturated bipolar

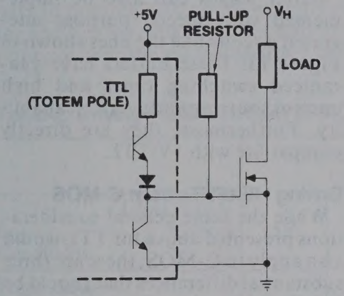
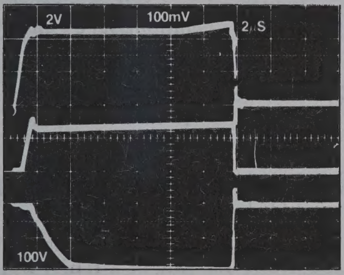


Figure 7. Direct Drive from TTL Output

Table 1. Driving HEXFETs from TTL (Totem Pole Outputs)

Logic Conditions	54/74	54H/74H	(54L)/ 74L	(54LS)/ 74LS	74S
Logic Zero Min. sink current for V_{OL}	16mA ≤0.4V	20mA ≤(0.4V)/	(2)/3.6mA ≤(0.3V)/ 0.4V	(4)/8 ≤(0.4V)/ 0.5V	20mA 0.5V
Logic One Max. source current for V_{OH}	-0.4mA ≥2.4V	-0.5mA ≥2.4V	-0.2mA ≥2.4V	-0.4mA ≥(2.5)/ 2.7V	-1.0mA ≥2.7V
Typical Gate Propagation Delay	10ns	7ns	50ns	12ns	4ns



Top Trace: Gate Voltage 2V/div.
Middle Trace: Drain Current 1A/div.
Bottom Trace: Drain Voltage 100V/div.
Time Scale: 2μs/div.

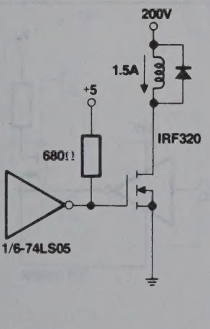
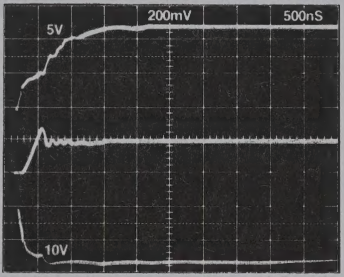


Figure 8. Waveforms Associated with a HEXFET Driven by a TTL Gate



Top Trace: Gate Voltage 5V/div.
Middle Trace: Drain Current 2A/div.
Bottom Trace: Drain Voltage 10V/div.
Time Scale: 500ns/div.

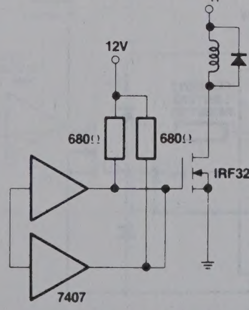


Figure 9. Waveforms Obtained with High Voltage TTL Driver

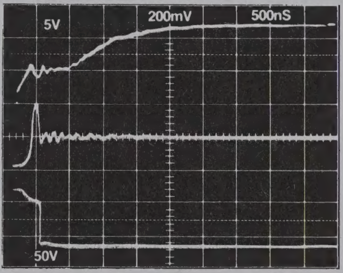


Figure 10. Waveforms Associated with the Circuit in Figure 9, at Different Drain Voltage. Same Scales except Bottom Trace: 100V/div.

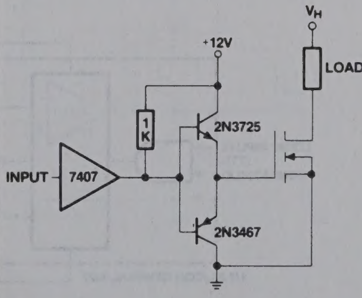


Figure 11. Simple Interface to Drive HEXFETs from TTL

transistor. The waveforms show also, that the device stays in the linear region for 9 microseconds and that, at the end of this time, the gate is finally free to rise to 5V, after the gate-to-drain capacitance has been fully charged. The main reason for such a poor performance is, of course, the fact that the maximum voltage available on the gate is 5V. The performance improves substantially if two or three gates are connected in parallel to charge or discharge this capacitance.

For guaranteed "saturation" and fast switching, high voltage open collector buffers can be used (7406, 7407, etc.), possibly with several devices connected in parallel.

Figure 9 shows the waveforms that can be obtained with two parallel high voltage drivers pulled up to 12V. Whilst a dramatic improvement can be seen with respect to Figure 8, the performance is still well below what can ultimately be obtained from a HEXFET. The waveforms in Figures 9 and 10 are for the same device, with the same drive circuit and the same drain current, but with different drain voltages. At higher voltages, C_{GD} takes a longer time to discharge, so the device stays in the linear region for more than 0.5 microseconds before reaching saturation.

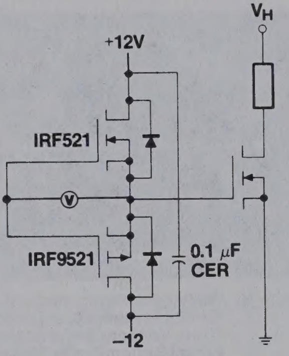


Figure 12. High Performance Driver

Whenever better switching performance is required, interface circuits should be added to provide fast current sourcing and sinking to the gate capacitances. One simple interface circuit is the one shown in Figure 11.

It is a complementary emitter follower stage, capable of sinking or sourcing approximately 1A. The choice of the output transistor is important when switching times have to be in the order of 40ns.

They should have good gain at high currents to be capable of delivering whatever current is required by the Miller effect during the allowed switching time. To gain a better insight on the operation of these transistors, we can attempt a rough calculation of the current they have to supply in a switching operation. Disregarding for a moment the Miller effect, if C_{GS} is 700pF (IRF330) and we want to charge it linearly to 12V in 40ns, a current pulse is required equal to:

$$I = \frac{C_{GS} \text{ X } V_{GS}}{t_s}$$

$$= \frac{0.7 \text{ X } 10^{-9} \text{ X } 12}{40.10^{-9}} = 0.21\text{A}$$

In the simplistic assumption that the gate-to-drain capacitance is discharged in the same time, assuming a drain voltage of 200V, we have:

$$I = \frac{C_{DG} \text{ X } V_{DS}}{t_s}$$

$$= \frac{40 \text{ X } 0.10^{-12} \text{ X } (200-12)}{40\ 10^{-9}} = 0.188\text{A}$$

In the final assumption that the two currents add up and that the switching frequency is 100kHz, we can obtain an approximate figure for the power lost in one driver transistor:

$$P = V_{CE} \text{ X } I_C \text{ X } t_s \text{ X } f = 1 \text{ X } 0.398 \text{ X } 40.10^{-9} \text{ X } 100\ 10^3 = 1.6\text{mW}$$

The conclusion is that the driver devices have to be capable of supplying 0.4A without significant voltage drop, but that hardly any power is dissipated in them. Core drivers (2N3725, 2N3244), seem to be the most suitable devices. Unfortunately, the gain of these devices drops very fast for currents over 0.5A. Audio drivers (2N5320, 2N5322), have better gain at high currents but are slower. A double buffer stage may be advisable in some applications with fast switching bipolar devices (2N-2369A and 2N4208 or MPS2369 and MPS3640) driving two HEXFETs, as shown in Figure 12.

Buffer stages can also be implemented with special purpose integrated circuits like the ones shown in Figure 13. These buffers have guaranteed switching times and high current sourcing and sinking capability. Furthermore, they are directly compatible with 5V TTL.

Driving HEXFETs from C-MOS

While the same general considerations presented above for TTL would also apply to C-MOS, there are three substantial differences that should be kept in mind:

1. C-MOS has a more balanced source/sink characteristic that, on a first approximation, can be thought of as a 500 ohm resistance for operation over 8V and a 1k ohm for operation under 8V (Table 2).
2. C-MOS can operate from higher supply voltages than 5V so that HEXFET saturation can be guaranteed.
3. Switching times are longer than TTL (Table 2).

When C-MOS outputs are directly coupled to the gate of a HEXFET, the dominant limitation to performance is not the switching time, but the internal impedance (assuming that C-MOS are operated from a 10V

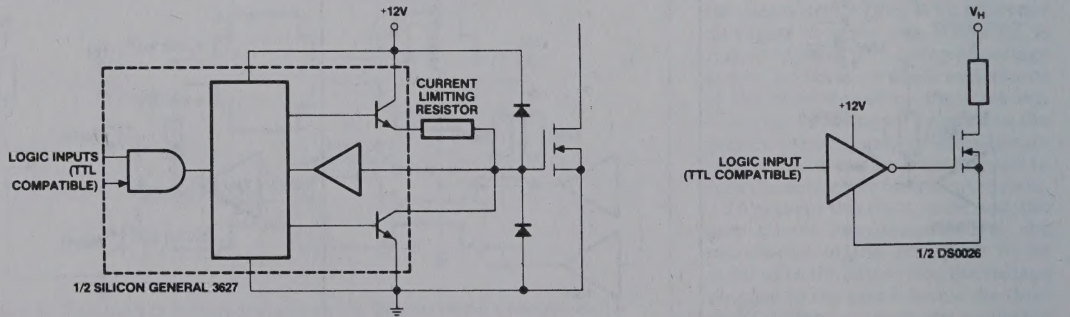


Figure 13. Buffer Stages Implemented with Special Purpose Drivers

or higher voltage supply). It will certainly not be able to turn OFF the HEXFET as fast as the TTL, while the turn-ON waveform will be slightly better than what can be achieved with a 7407 with a 680 ohm pull-up resistor. Of course, gates can be paralleled in any number to lower the impedance and this makes C-MOS a very simple and convenient means of driving HEXFETs. Drivers can also be used, like the 4049 and 4050 which have a much higher current sinking capability (Table 2), but they do not yield any significant improvement in current sourcing.

For better switching speeds, buffer circuits should be considered, not only to provide better current sourcing and sinking capability, but also to improve over the switching times of the C-MOS output itself. The circuit shown in Figure 11 (without the pull-up resistor which would not be needed), and Figure 12 will improve the drive capability, while the circuits in Figure 13 will improve both drive capability and switching times, but require a TTL compatible drive signal (5V). Another possibility, of course, is to interface C-MOS to TTL and then use the TTL drive circuits.

Driving HEXFETs From Linear Circuits

The complementary emitter follower configuration of Figure 11 can also be used in linear applications to improve drive capability from an op-amp or other analog source (Figure 14).

Table 2. Driving HEXFETs from C-MOS (Buffered)

	Standard Buffered Outputs			4049/4050 Drivers		
Logic Conditions / Logic Supply Voltage	5V	10V	15V	5V	10V	15V
Logic Zero: Approximate sink current for $V_{OL} \leqslant 1.5V$	1.5mA	3.5mA	4mA	20mA	40mA	40mA
Logic One: Minimum source current for V_{OH}	-0.51mA $\geqslant$4.6V	-1.3mA $\geqslant$9.5V	-3.4mA $\geqslant$13.5V	-1.25mA $\geqslant$2.5V	-1.25mA $\geqslant$9.5V	-3.75mA $\geqslant$13.5V
Typical switching times of logic drive signals: RISE FALL	 100ns 100ns	 50ns 50ns	 40ns 40ns	 100ns 40ns	 50ns 20ns	 40ns 15ns

If the driving signal is generated by an operational amplifier, the use of power operational amplifiers (e.g., μA791) that can supply as much as 1A can be considered. In practice, their slew rate is so low (0.5V/μs) that their current capability would be redundant and the usable bandwidth would be less than 25kHz. A larger bandwidth can be obtained with better operational amplifiers followed by a current booster, like the ones shown in Figures 15 or 16. For a system bandwidth of 1MHz, the op-amp bandwidth must be significantly higher than 1MHz and its slew rate at least 30V/μs. Presently, there are several devices capable of this performance, e.g., LF157, LM110, μA715, HA2620, etc. If a larger bandwidth is needed, special purpose current amplifiers can be used, like the HA2630 (bandwidth 8MHz, slew rate 500V/μs, 0.4A output current) or very fast operational amplifiers like the NE5539 (bandwidth 48MHz, slew rate 600V/μs) followed by a current booster.

When analog signals determine the switching frequency or duty cycle of a HEXFET, as in PWM applications, a voltage comparator is normally used to command the switching. Here, too, the limiting factors are the slew rate of the comparator and its current drive capability. Response times under 40ns can be obtained at the price of low output voltage swing (TTL compatible) and this implies the use of output buffers like the ones shown in Figures 9, 11, 12 and 13. If better switching speeds

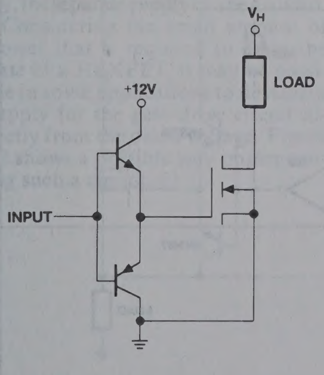


Figure 14. Current Booster for Analog Applications

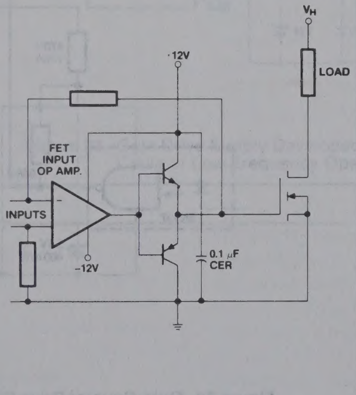


Figure 15. Dual Supply Op-Amp Drive Circuit

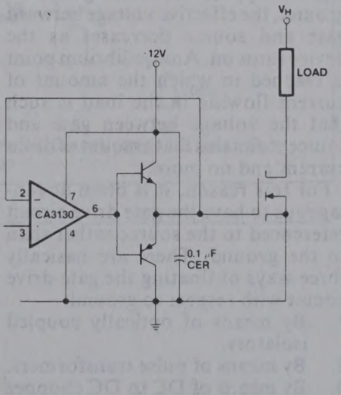


Figure 16. Single Supply Op-Amp Drive Circuit (Voltage Follower)

are desired, a fast op-amp should be used. Figure 17 shows a typical comparator connection.

In many applications, when the HEXFET is turned on, current transfers from a freewheeling diode into the HEXFET. If the switching speed is high and the stray inductances in the diode path are small, this transfer can occur in such a short time as to cause a reverse recovery current in the diode high enough to destroy it. For this reason, it may be necessary to slow down the turn-on of the HEXFET while leaving the turn-off as fast as practical. Pulse shaping circuits can be used for this purpose, like the ones in Figures 18 and 19.

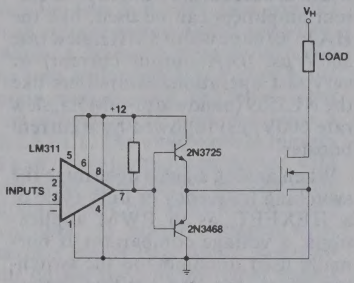


Figure 17. Comparator Drive

In linear applications, the use of special circuits like the LM391 audio driver with an output booster can be considered. The LM391 has separate source and sink outputs.

Drive Circuits Not Referenced to Ground

To drive a HEXFET into saturation, an appropriate voltage must be applied between the gate and source. If the load is connected between source and ground, and the drive voltage is applied between gate and ground, the effective voltage between gate and source decreases as the device turns on. An equilibrium point is reached in which the amount of current flowing in the load is such that the voltage between gate and source maintains that amount of drain current and no more.

For this reason, it is often advantageous to have the gate drive circuit referenced to the source rather than to the ground. There are basically three ways of floating the gate drive circuit with respect to ground:

1. By means of optically coupled isolators.
2. By means of pulse transformers.
3. By means of DC to DC chopper circuits with transformer isolation.

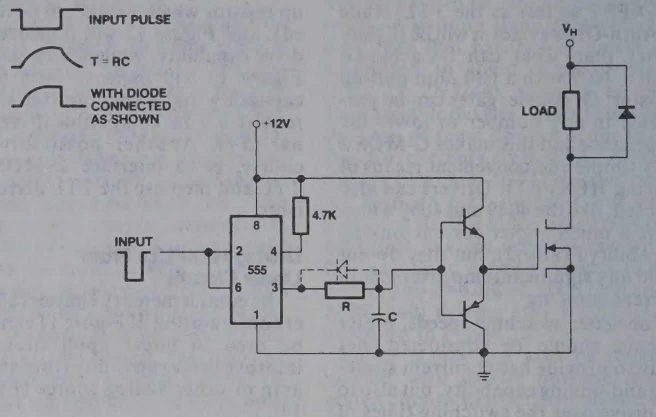


Figure 18. 555 as Schmitt Trigger in a Pulse Shaping Application

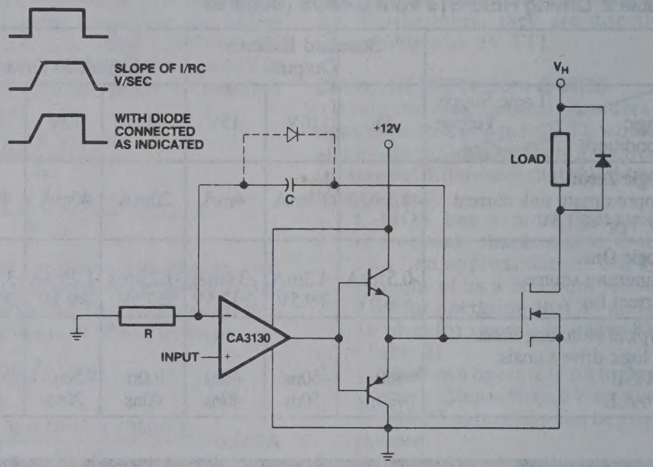


Figure 19. Pulse Shaper

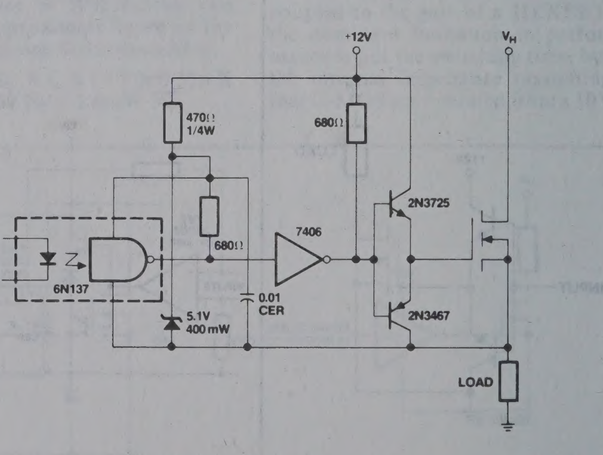


Figure 20. Opto Coupler Drive Circuit

Opto couplers require a separate supply grounded to the source on the receiving end of the optical link. Optically coupled gates (TTL compatible) are available with 50ns delay times and 25ns rise and fall times. They can be used to a few MHz, but they require a booster stage at the output, as shown in Figure 20. C-MOS level translators, like the 4504, could be used in place of the 7406. If speed is not a major factor, a simplified circuit can be used like the one shown in Figure 21.

The Schmitt trigger function of the 74C14 could be accomplished with a 555, which has fairly good switching and driving capabilities (100ns, 0.2A).

One of the major difficulties encountered in the use of opto couplers is their susceptibility to noise. This is of particular relevance in applications where high currents are being switched rapidly. They do, however, offer a simple means of transmitting a signal that contains a DC component. Pulse transformers, on the other hand, can only transfer to the secondary the AC component of the input signal. Consequently, their output voltage swings from negative to positive by an amount that changes with the duty cycle. Furthermore, whatever leakage inductance the transformer has, reduces its effectiveness as a gate drive circuit. To overcome these difficulties, a signal conditioning stage may be necessary; this requires a separate power supply. It remains, however, a reliable approach with high noise immunity, whenever the duty cycle has a fixed known minimum.

Chopper circuits are fairly complex, expensive and limited in bandwidth and performance. They do have their advantages, though, like the possibility of transferring a DC component, noise immunity and the fact that with some additional circuitry, the separate supply can be avoided.

Considering the small amount of power that is required to drive the gate of a HEXFET, it may be possible in some applications to develop a supply for the gate drive circuit directly from the drain voltage. Figure 22 shows a possible way implementing such a circuit. ☐

If the duty cycle is small, or the frequency is low, the circuit in Figure 23 should be considered. The size of Q, R, and C depend on the duty cycle of the drain voltage waveform as well as its frequency and the amount of gate capacitance that has to be driven.

Obviously, this circuit will not work if the HEXFET may be kept in the on-state for an undetermined period of time and there is lower frequency limit below which C becomes quite large and the circuit is not attractive any longer. ☐

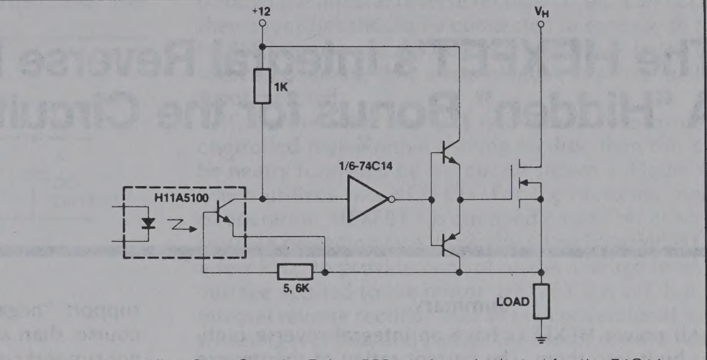


Figure 21. Simplified Opto Coupler Drive. 555 can be substituted for the 74C14

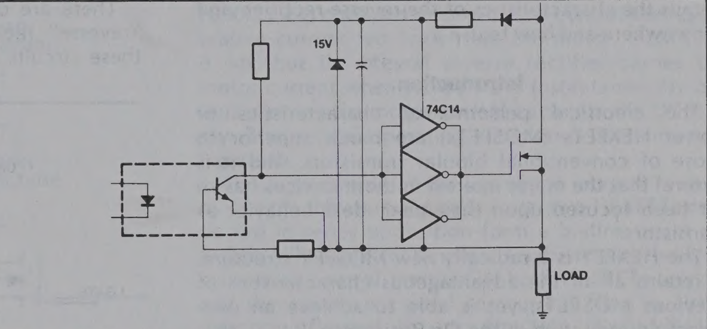


Figure 22. Supply for the Gate Drive Circuit Developed from the Drain Voltage

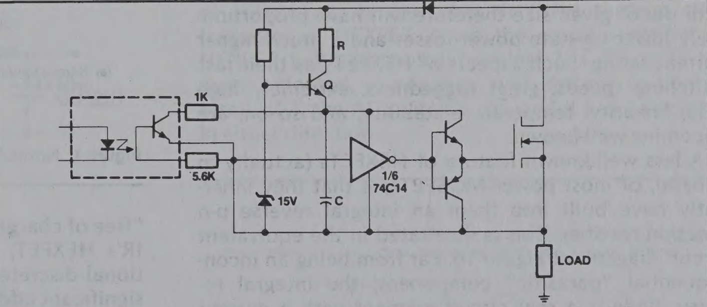


Figure 23. Gate Drive Supply Developed from the Drain Voltage for Small Duty Cycle or Low Frequency Operation

CHAPTER 5

APPLICATION NOTE 934

The HEXFET's Integral Reverse Rectifier — A "Hidden" Bonus for the Circuit Designer

Summary

All power HEXFETs have an integral reverse rectifier built into them. The current rating of the reverse rectifier is equal to that of the transistor. This article details the characteristics of the reverse rectifier, and shows where and how to use it.

Introduction

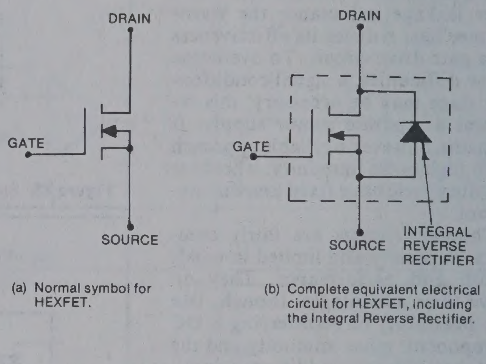
The electrical performance characteristics of power HEXFETs (MOSFETs) are much superior to those of conventional bipolar transistors, and it is natural that the major interest in these devices has so far been focused upon their near ideal behavior as transistors.

The HEXFET is a radically new MOSFET structure. It retains all of the advantageous characteristics of previous MOSFETs, yet is able to achieve an over threefold reduction in the On-Resistance, $R_{DS(on)}$, in a transistor die of given dimensions. A HEXFET transistor die of given size therefore will have proportionately lower on-state power losses and a much higher current rating. Such aspects of HEXFETs as their fast switching speeds, great ruggedness, extremely high gain, linearity, temperature stability, and so on, are becoming well-known.

A less well-known feature of HEXFETs (actually in general, of most power MOSFETs) is that they inherently have built into them an integral reverse p-n junction rectifier. This is illustrated in the equivalent circuit diagram of Figure 1b. Far from being an inconsequential "parasitic" component, the integral reverse diode is a real circuit element with a current handling capability as high as that of the transistor itself.

The integral reverse rectifier may or may not be important in a practical circuit. In some applications it is irrelevant, because the circuit operation is such that the voltage across the transistor never reverses; hence, the forward conduction characteristic of the diode never comes into play. Other circuits require the switching device to support "negative" voltage as well as "positive" voltage. In that event, a rectifier must be connected in series with the HEXFET, because the integral reverse diode does not allow it to support "negative" voltage. This is no different, of course, than with a bipolar transistor, which also cannot support significant reverse voltage (but, unlike the HEXFET, nor can it carry significant reverse current).

There are other circuits which actually require a "reverse" rectifier across the switching device. In these circuits, it will often be possible to utilize the "free of charge" the integral reverse rectifier built into IR's HEXFET, thereby obviating the need for additional discrete rectifiers in the circuit. This can be a significant added bonus of using the HEXFET.



(a) Normal symbol for HEXFET.

(b) Complete equivalent electrical circuit for HEXFET, including the Integral Reverse Rectifier.

Figure 1. Normal and Complete Symbols for the HEXFET

The purpose of this application article is to discuss some of the uses, as well as the characteristics, ratings and limitations of the integral reverse rectifier in IR's HEXFETs. Specific solutions to the potential circuit problems will be considered, and specific design procedures given. The intention is to give the circuit designer the information he needs to assess the importance and applicability of this "hidden" component in IR's HEXFETs.

Some Basic Circuit Applications

The following discussion deals with various circuit examples; this will give a basic understanding of where the reverse rectifier is important, and where it can be utilized.

First, there are circuits in which the reverse rectifier has no effect. The fly-back converter shown in Figure 2a is an example. Here, the voltage across the HEXFET is always positive; the integral reverse rectifier plays no part in the circuit operation, and it stays unobtrusively in the background. The same is true in the "forward" converter circuit, shown in Figure 2b. There are many circuits of this type.

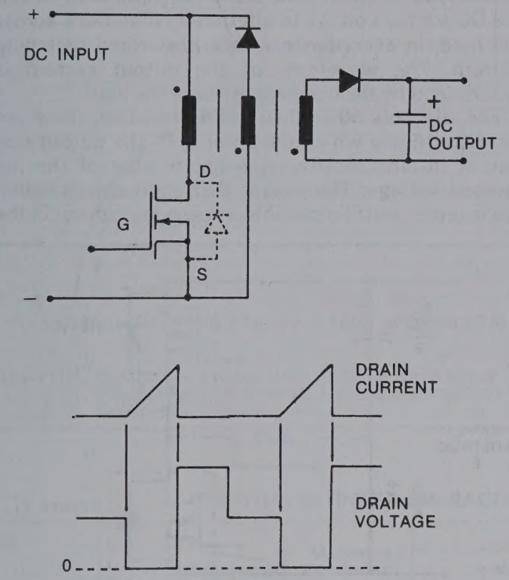


Figure 2a. Flyback Converter Circuit

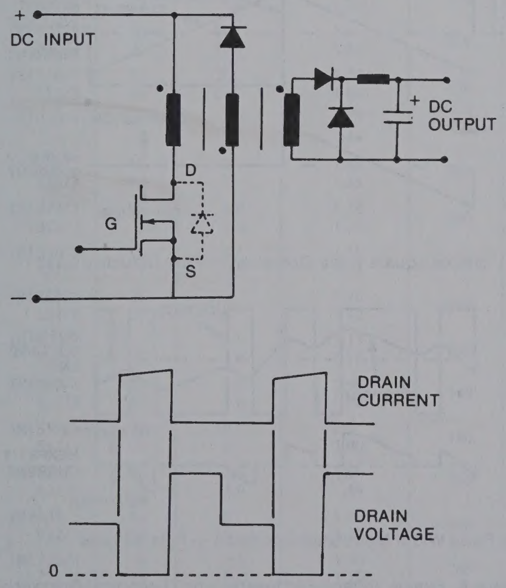


Figure 2b. Forward Converter Circuit

The integral reverse rectifier has no obvious effect upon the operation of the DC to DC chopper circuit shown in Figure 3. If a situation could arise, however, where the motor is driven at overspeed by an "overhauling" load, "uncontrolled" current would flow through the integral reverse rectifier. If this can occur, then a rectifier should be connected in series with the HEXFET, to prevent the flow of energy back to the DC source, assuming that a regenerative braking facility is not required.

If, on the other hand, it is required to provide a controlled regenerative braking facility, then this can be neatly furnished by the circuit shown in Figure 4a, which utilizes two HEXFETs. For the motoring mode of operation, HEXFET 1 is chopped on and off at some suitable repetition rate, typically a few hundred Hz to a few kHz, to provide control of the average level of voltage applied to the motor. HEXFET 2 is off, but its integral reverse rectifier acts as the conventional freewheeling rectifier, and carries the motor current when HEXFET 1 is instantaneously off.

For the regenerative braking mode of operation, HEXFET 2 is chopped on and off, to control the regenerative current fed back from the motor. HEXFET 1 is off, but its integral reverse rectifier carries the motor current when HEXFET 2 is instantaneously off, thus carrying the motor current back into the DC supply. Theoretical operating waveforms are shown in Figure 4b.

Another example of the use of the integral reverse rectifier is shown in Figure 5. Here, two HEXFETs connected in series opposition form a bi-directional AC switch. When control terminal 3 is driven positive with respect to control terminal 4, both HEXFETs are on, and the switch is closed for current flow in either direction. Current in one direction flows via the transistor of HEXFET 1 and the reverse rectifier of HEXFET 2; in the other, it flows through the transistor of HEXFET 2 and the reverse rectifier of HEXFET 1. When control terminal 3 is driven to the same potential, or negative, with respect to control terminal 4, the AC switch is off, and it blocks voltage in either direction.

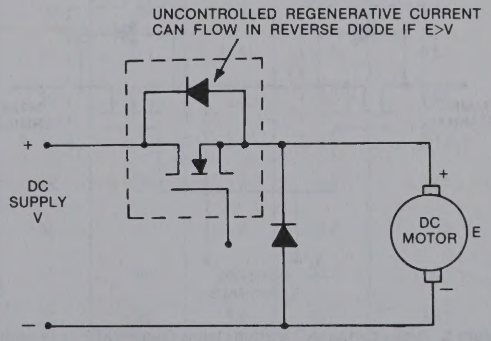

UNCONTROLLED REGENERATIVE CURRENT CAN FLOW IN REVERSE DIODE IF E>V
+
DC SUPPLY V
−
+
DC MOTOR
E
−

Figure 3. DC Chopper Circuit for Motor Speed Control

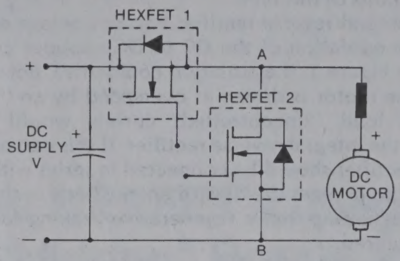


Figure 4a. HEXFET Circuit for Providing Speed Control and Regenerative Braking of DC Motor

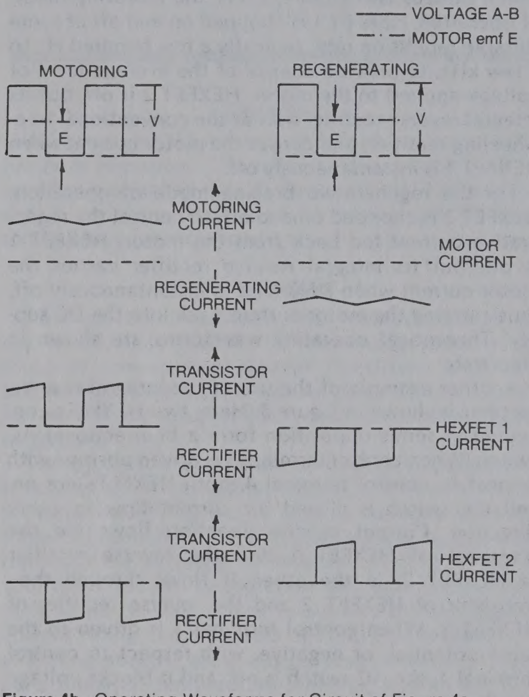


Figure 4b. Operating Waveforms for Circuit of Figure 4a.

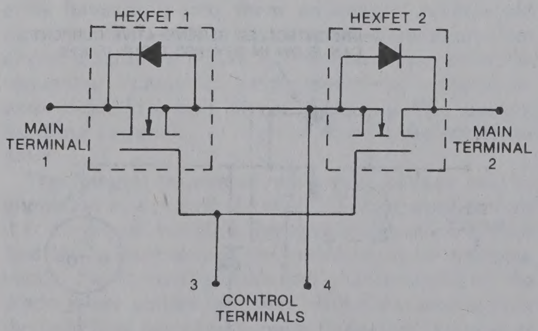
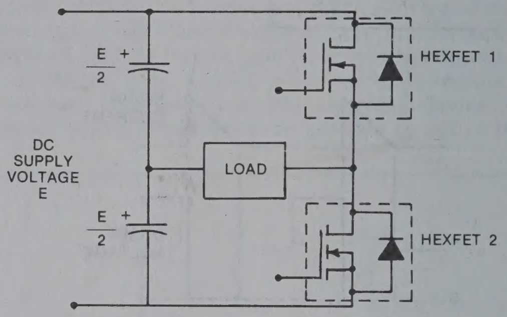


Figure 5. Bidirectional AC Switch Using Two HEXFETs in Series Opposition

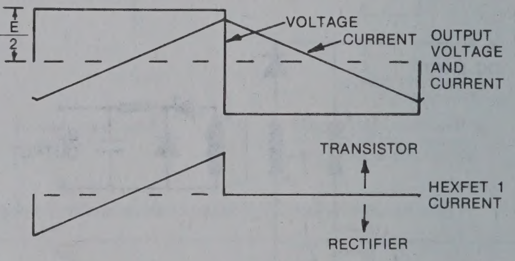
The attractive feature of this AC switch circuit is that a common drive signal serves both HEXFETs. Thus the designer is not faced with the need to furnish two separate, isolated drive signals.

Perhaps the most obvious use of the integral reverse rectifier built into IR's HEXFETs is in voltage-fed DC to AC inverter circuits of the types commonly used for switching power supplies, motor speed controllers, and general purpose AC power supplies. In these types of circuit, the basic principle is to switch the DC supply voltage in alternating directions across the load, in accordance with a prescribed switching pattern. The waveform of the output current is determined by the characteristics of the load.

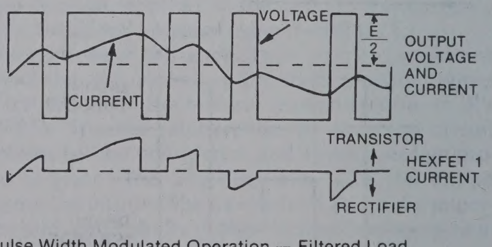
For all loads other than purely resistive, there are intervals during which the polarity of the output current is instantaneously opposite to that of the impressed voltage. This means that each switch within the inverter must be capable of carrying current in the



(a) Voltage-Fed Inverter Circuit



(b) Simple Square Wave Operation — Pure Inductive Load



(c) Pulse Width Modulated Operation — Filtered Load

Figure 6. Simple Voltage-Fed Inverter and Theoretical Operating Waveforms

"reverse" direction. In a conventional inverter circuit, this facility is provided by connecting a reverse rectifier across each switching device. These rectifiers are often known as "reactive feedback" rectifiers.

The integral reverse rectifier in the HEXFET can automatically serve as the reactive feedback rectifier.

A simple "half bridge" DC to AC inverter circuit operating from a "split" DC supply is shown in Figure 6a. The circuit can be operated in a simple square wave mode, in which case a single voltage pulse is produced for each half cycle of the output, or it can be operated in a more complex "multi-pulse" mode,

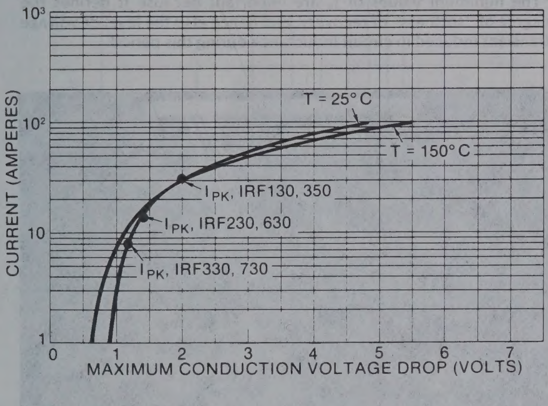


Figure 7(a). Conduction Voltage Drop vs. Current in Integral Reverse Rectifier (IRF130, 230, 330, 530, 630, 730 Series HEXFET

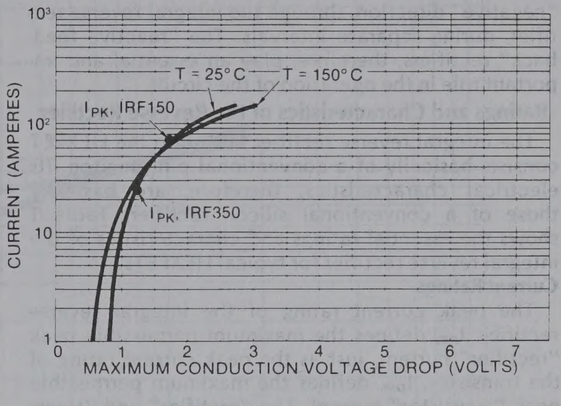


Figure 7(b). Conduction Voltage Drop vs. Current in Integral Reverse Rectifier (IRF150 and 350 Series HEXFET)

TABLE 1
ESSENTIAL RATINGS & CHARACTERISTICS OF THE INTEGRAL REVERSE RECTIFIER

HEXFET Series	Peak Current Rating I_{PK} Amps	Continuous Direct (And RMS) Current Rating	Maximum Conduction Voltage Drop At I_{PK}, T = 25°C Volts	RECTIFIER RECOVERY Initial Forward Rectifier Current = I_{PK}, di/dt = 100A/μs						Thermal Resistance
				$t_{a(max)}$ Nanoseconds		$t_{b(min)}$ Nanoseconds		$Q_{RR(MAX)}$ μC		J-C
				T = 25°C	T = 150°C	T = 25°C	T = 150°C	T = 25°C	T = 150°C	°C/W
IRF120/1 122/3	15 12	6.0 5.0	1.90 1.70	140	200	15	25	2.0	4.0	3.12
IRF130/1 132/3	30 25	12 10	2.0 1.80	180	290	35	55	2.0	5.1	1.67
IRF150/1 152/3	70 60	28 24	1.70 1.60	210	335	65	100	3.7	9.5	0.83
IRF220/1 222/3	10 8	4.0 3.5	1.57 1.44	350	500	30	50	6.0	12.0	3.12
IRF230/1 232/3	15 12	7 6	1.45 1.31	360	575	60	100	8.1	20.8	1.67
IRF320/1 322/3	6 5	3.0 2.5	1.30 1.25	280	400	25	40	5.0	10.0	3.12
IRF330/1 332/3	8 7	4 3.5	1.15 1.13	295	470	60	95	5.9	15.1	1.67
IRF350/1 352/3	25 20	11 10	1.20 1.12	600	960	85	135	22.5	57.6	0.83
IRF430/1 432/3	7 6	3.5 3.0	1.13 1.10	260	420	50	80	5.5	14.0	1.67
IRF520/1 522/3	15 12	5.0 4.0	1.90 1.70	140	200	15	25	2.0	4.0	3.12
IRF530/1 532/3	30 25	10 8	2.0 1.80	180	290	35	55	2.0	5.1	1.67
IRF620/1 622/3	10 8	3.5 3.0	1.57 1.44	350	500	30	50	6.0	12.0	3.12
IRF630/1 632/3	15 12	6 5	1.45 1.31	360	575	60	100	8.1	20.8	1.67
IRF720/1 722/3	6 5	2.5 2.0	1.30 1.20	280	400	25	40	5.0	10.0	3.12
IRF730/1 732/3	8 7	3.5 3.0	1.15 1.13	295	470	60	95	5.9	15.1	1.67

with many voltage pulses being produced for each fundamental output half cycle. This latter technique significantly reduces the harmonic distortion at the output.

These two operating techniques are illustrated by the waveforms in Figures 6b and 6c respectively. These waveforms show that current flows both in the "positive" direction, through the transistor, and in the "negative" direction, through the integral reverse rectifier, during separate intervals. The "reactive feedback" rectifiers, therefore, play an essential and important role in the operation of the circuit.

Ratings and Characteristics of the Reverse Rectifier

The integral reverse rectifier built into the HEXFET consists basically of a conventional p-n junciton. Its electrical characteristics, therefore, are basically those of a conventional silicon rectifier. Table 1 shows the essential ratings and characteristics of the integral reverse rectifier for typical HEXFETs.

Current Ratings

The peak current rating of the integral reverse rectifier, I_{PK}, defines the maximum permissible peak "rectifier" current, just as the peak current rating of the transistor, I_{DM}, defines the maximum permissible peak "transistor" current. The "rectifier" and "transistor" peak current ratings are the same as one another, as also are the RMS ratings.

Conduction Voltage

Relationships between the conduction voltage drop of the integral rectifier and the instantaneous current through it, at junction temperatures of 25°C and 150°C, are shown in Figure 7. The rated pulsed current level, I_{PK}, is indicated for reference on these diagrams. With a current equal in value to I_{PK} the voltage drop across the integral reverse rectifier is relatively low, in the region of 1 to 2V.

A point of theoretical interest is that the conduction voltage drop of the integral reverse rectifier can be modified by applying positive drive voltage to the gate of the HEXFET. Figure 8 shows what happens as the gate to source voltage is increased. At low current levels, the conduction voltage drop across the rectifier decreases as the drive voltage is increased.

The physical explanation for this is simple. As the gate voltage is increased, the channel resistance of the transistor reduces due to the applied electric field, just as it does for the normal "transistor" direction of current flow. The reverse rectifier is thus shunted by the channel resistance, and the equivalent circuit is as shown in Figure 9.

At low current levels, the voltage drop across the channel resistance is lower than it would be across the rectifier on its own, and most of the current flows through the equivalent resistor. As the current is increased, the voltage drop across the rectifier is lower than it would be across the resistor on its own; most of the current now flows through the rectifier. The resistor then has little effect, and the influence of the applied gate drive voltage is minimal.

Reverse Recovery

An important practical consideration is the reverse recovery characteristic of the integral reverse rectifier. This rectifier is a conventional p-n junction, and therefore it exhibits a classical reverse recovered charge; that is to say, when the rectifier switches off, the current through it reverses for a short period, as illustrated in Figure 10.

Table 1 shows maximum values of T_a and minimum* values of t_b for an initial rectifier conduction current of I_{PK}, and a rate of change of current (di/dt) of 100A/μs. Values of t_a and t_b for other values of initial

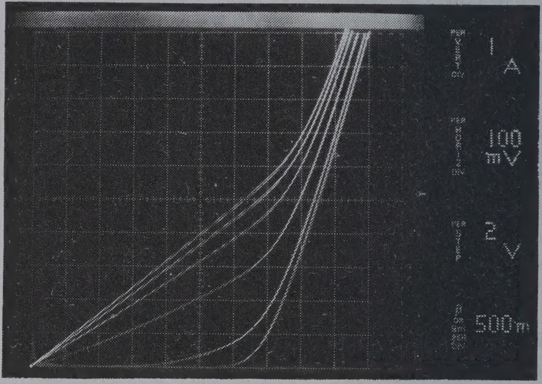
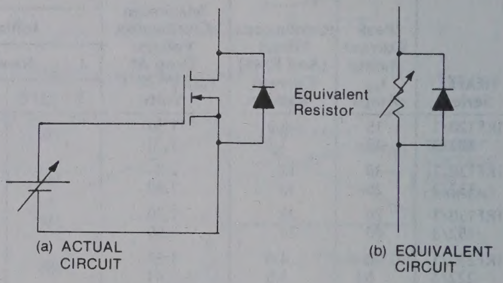


Figure 8. Typical Curves of forward conduction voltage vs. current through integral reverse rectifier, with varying amounts of applied gate-source voltage. IRF130 V_{GS} = 0, + 2, + 4, + 6, + 8, + 10V.



(a) ACTUAL CIRCUIT

(b) EQUIVALENT CIRCUIT

Figure 9. Varying applied gate voltage results in varying equivalent resistor across reverse rectifier.

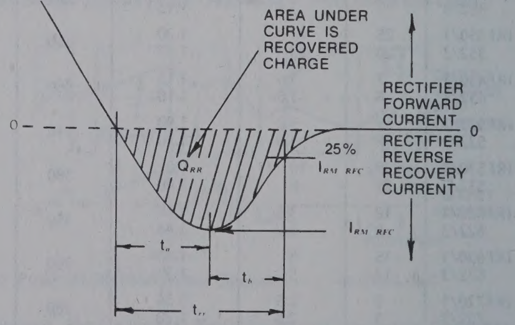

AREA UNDER CURVE IS RECOVERED CHARGE
RECTIFIER FORWARD CURRENT
0
0
RECTIFIER REVERSE RECOVERY CURRENT
25%
$I_{RM\ REC}$
Q_{RR}
$I_{RM\ REC}$
t_a
t_b
t_{rr}

Figure 10. Rectifier Reverse Recovery

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*The minimum values of t_b are important because it defines the degree of "softness" of recovery, and hence also the level of voltage transient induced in circuit inductance during this period.

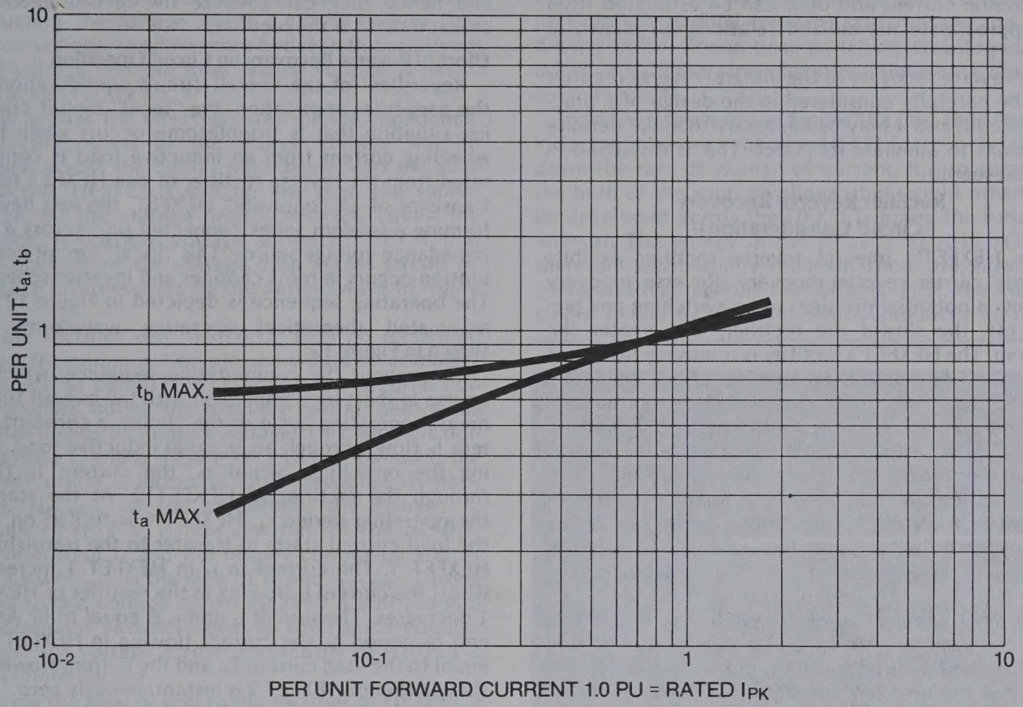


Figure 11a. Approximate correction factors for t_a and t_b as function of per unit initial forward rectifier current

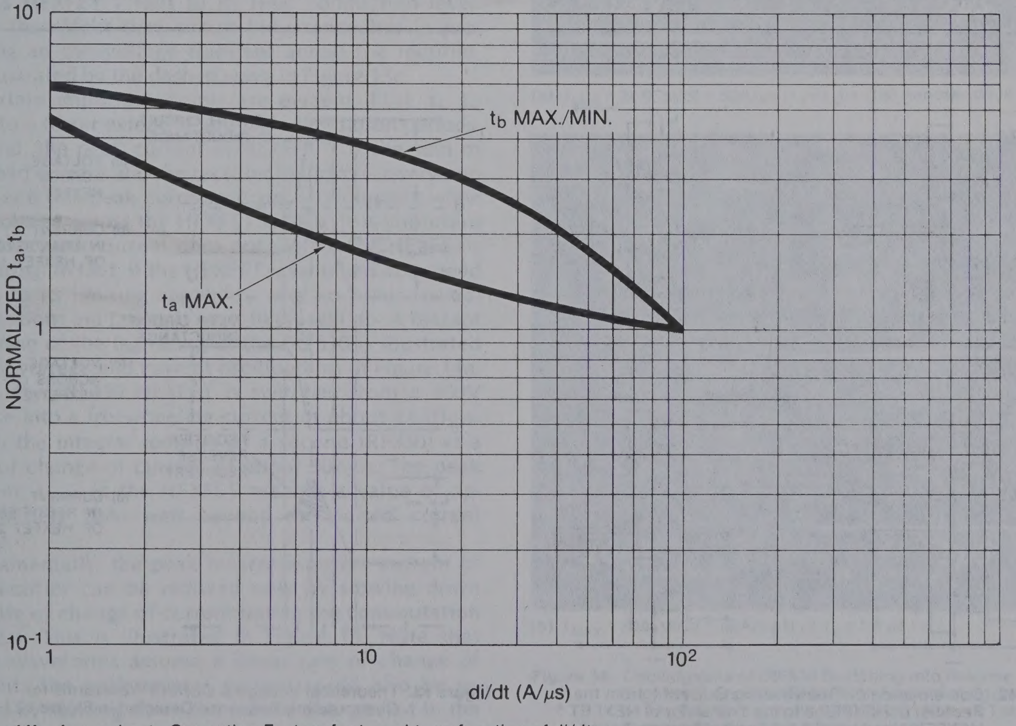


Figure 11b. Approximate Correction Factors for t_a and t_b as function of di/dt

conduction current and di/dt can be estimated from the approximate normalized relationships shown in Figure 11

The reverse recovery of the integral reverse rectifier must be carefully considered in the design of a practical circuit, and it may be necessary to make definite provisions to alleviate its effect. This is discussed in the next section.

Rectifier Reverse Recovery -Circuit Considerations-

The HEXFET's integral reverse rectifier exhibits minority carrier reverse recovery. Reverse recovery presents a potential problem when switching any rectifier off; the slower the rectifier, the greater the problem. The HEXFET's rectifier is relatively fast—not as fast as the fastest discrete rectifiers available, but considerably faster than comparably related conventional general purpose rectifiers. By comparison with the HEXFET itself, on the other hand, the switching speed of the integral reverse rectifier is quite slow. The switching speed of a circuit utilizing the reverse rectifier of the HEXFET may therefore be limited by the rectifier. Whether this will be so depends upon the circuit and the operating conditions, as discussed later.

The most common applications of the HEXFET in which the switching speed, and hence frequency, will potentially be limited by the rectifier, are DC to DC choppers and inverters for regulated power supplies, electric motor controllers, and so on, in which "multiple" voltage pulses are used. Fortunately, these applications generally do not require ultra fast switching, and hence they can tolerate the reverse recovery characteristic of the rectifier.

Effect of Reverse Recovery on Circuit Operation

Regardless of the overall circuit configuration, or the particular application, the "local" circuit operating situation that is troublesome occurs when freewheeling current from an inductive load is commutated from the reverse rectifier of one HEXFET to the transistor of an "opposite" HEXFET, the two devices forming a tandem series connected pair across a low impedance voltage source. This "local" circuit configuration occurs in most chopper and inverter schemes. The operating sequence is depicted in Figure 12 and associated theoretical operating waveforms are shown in Figure 13.

Throughout the commutating sequence, which of course is short by comparison with the overall fundamental operating cycle of the circuit, a constant current I_o flows through an external inductive load. During the operating period t_o, the current I_o flows through the rectifier of HEXFET 2. At the start of the operating period t_1, HEXFET 1 is turned on, and the load current starts to transfer to the transistor of HEXFET 1. The current in i_1 in HEXFET 1 increases, whilst the current i_2 flowing in the rectifier of HEXFET 2 decreases. The sum of i_1 and i_2 is equal to I_o. At the end of period t_1, the current flowing in HEXFET 1 is equal to the load current I_o, and the current flowing in the rectifier of HEXFET 2 is instantaneously zero.

Note that during period t_1 (also during the subsequent period t_a) the voltage across HEXFET 1 theoretically is virtually the full source voltage. This is be-

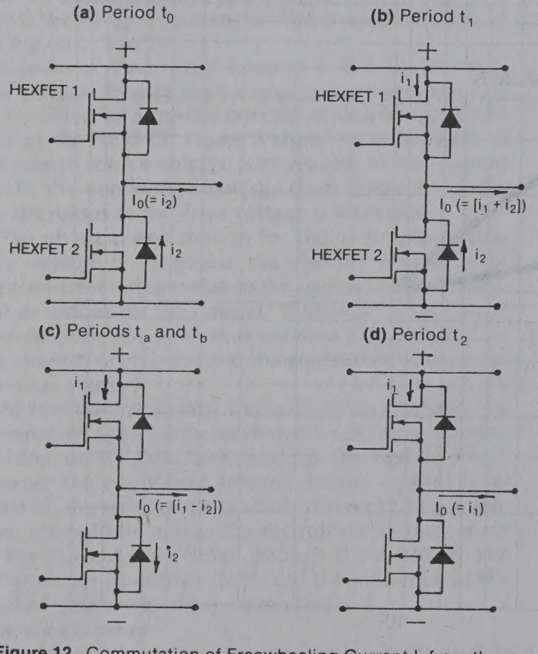


Figure 12. Commutation of Freewheeling Current I_o from the Rectifier of HEXFET 2 to the Transistor of HEXFET 1. HEXFET 1 and HEXFET 2 Form a Tandem Series Connected Pair Across a DC Source.

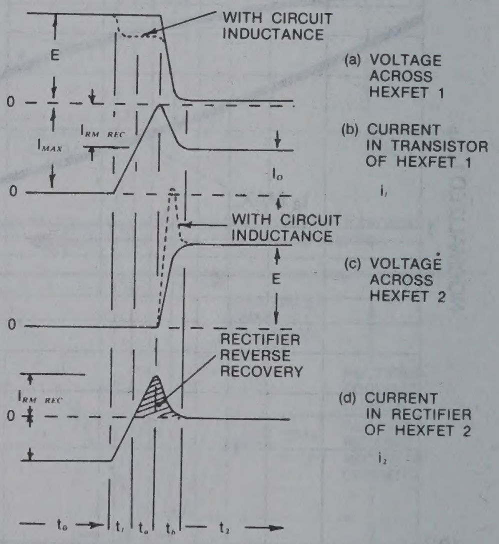

WITH CIRCUIT INDUCTANCE
E
0
(a) VOLTAGE ACROSS HEXFET 1
I_{MAX}
$I_{RM\ REC}$
I_o
(b) CURRENT IN TRANSISTOR OF HEXFET 1
i_1
0
WITH CIRCUIT INDUCTANCE
E
(c) VOLTAGE ACROSS HEXFET 2
0
RECTIFIER REVERSE RECOVERY
$I_{RM\ REC}$
0
(d) CURRENT IN RECTIFIER OF HEXFET 2
i_2
t_o
t_1
t_a
t_b
t_2

Figure 13. Theoretical Voltage & Current Waveforms for Commutating Sequence Depicted in Figure 12.

cause so long as the rectifier of HEXFET 2 remains conducting, the voltage across it can be only its conduction voltage; the difference between this relatively small voltage and the total source voltage is developed across HEXFET 1.

This ignores the effect of stray circuit impedance. In practice, some of the source voltage will be dropped across the circuit impedance, and the voltage across HEXFET 1 will be less than the source voltage, by the voltage drop across the circuit impedance. A possible voltage across HEXFET 1 that takes account of the voltage drop across circuit inductance is represented by the dashed wave in Figure 13a.

If the rectifier was "perfect," with no recovered charge, the commutation process would be complete at the end of period t_1. In practice, the rectifier current reverses during the recovery period, before the rectifier begins to support voltage. This happens during periods t_a and t_b (Figure 12c). During period t_a the reverse current i_2 increases until it reaches its peak value, $I_{RM(REC)}$. In the meantime, the current i_1, through HEXFET 1, is now the sum of the rectifier reverse current i_2 and the output current I_O, and its peak value, I_{MAX}, is the sum of I_O and $I_{RM(REC)}$. During period t_a, the voltage across HEXFET 1 still theoretically remains virtually equal to the source voltage, because the voltage across the rectifier of HEXFET 2 is still relatively low.

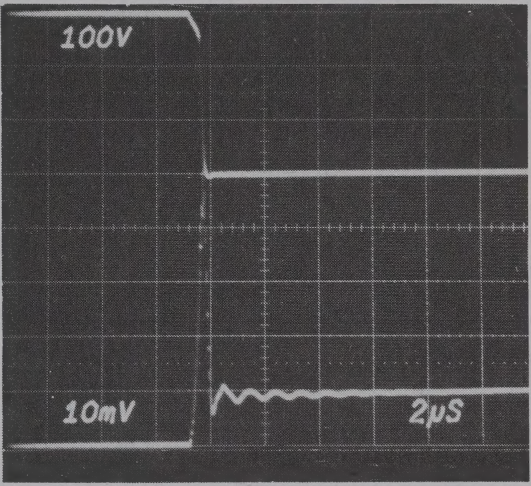
During the final period t_b, the rectifier of HEXFET 2 begins to support reverse voltage. The reverse rectifier recovery current i_2 decreases, and the voltage across HEXFET 1 falls to its final conduction level. Note the effect that circuit inductance has in producing an overvoltage transient across the rectifier, as illustrated by the dashed wave in Figure 13c.

Certain important points are evident. First, t_1, t_a, and, to a lesser extent, t_b, are high dissipation periods. Second, the peak current in HEXFET 1 is the sum of the load current and the rectifier reverse recovery current, and this peak current occurs at an instant when the voltage across the HEXFET is high. It is important that this peak current does not violate the HEXFET's I_{DM} rating. In fact, if the HEXFET is switched at a speed close to its limiting capability, and no other special precautions are taken, it most likely will do. A blatant violation of the I_{DM} rating of the IRF330 is illustrated by the voltage and current oscillograms in Figure 14a. Here, the IRF330 HEXFET is switched from a 300V source into a freewheeling current of about 4A (flowing in the integral rectifier of a second IRF330) at a rate of change of current of about 50A/μs. The peak current, I_{MAX}, in the HEXFET reaches a value of approximately 20A—well beyond the pulsed current rating.

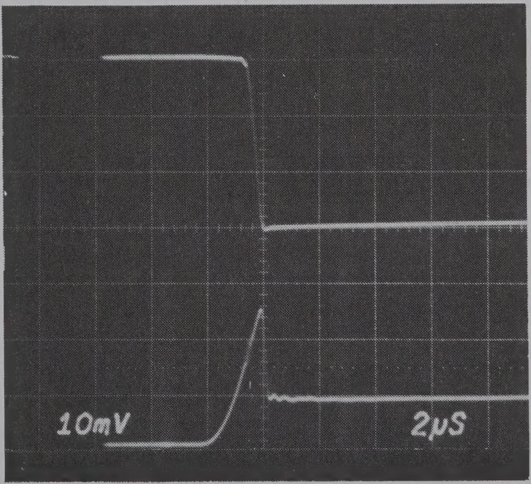
Fundamentally, the peak reverse recovery current of the rectifier can be reduced only by slowing down the rate of change of current during the commutation process. This is illustrated in Figure 15. Note that these waveforms assume a linear rate of change of current. The peak reverse current could also be reduced by slowing down the rate of change just in the reverse recovery region.

The rate of change of current can be controlled either by inserting inductance into the circuit, or by purposefully slowing down the rate of rise of the gate driving pulse. Theoretical switching waveforms obtained with these alternative techniques are illustrated in Figure 16.

From the waveforms in Figure 16a, it is seen that an inductor in series with the HEXFET not only slows down the rate of change of current, it also supports the bulk of the source voltage, that would otherwise be developed across the HEXFET during the turn-ON interval. The energy in the HEXFET at switch-ON is therefore substantially reduced. There are, however, some disadvantageous side effects. First, the energy stored in the inductor inherently produces an over-



(a) I_{MAX} = 20A, di/dt = 50A/μs ($t_1 + t_a$) = 300 nanoseconds



(b) I_{MAX} = 20A, di/dt = 50A/μs ($t_1 + t_a$ = 1.8 μs

Figure 14. Oscillograms of IRF330 Switching into Reverse Rectifier of Another IRF330 with Freewheeling Current of 4A. Top Trace: Voltage 100V/div. Bottom Trace: Current 4A/div. Time Scale: 2 μs/div.

voltage transient when the rectifier recovers, as shown. This voltage transient must be limited by an RC snubber or a voltage clamp, which dissipates the stored energy. Second, the inductance creates an overvoltage transient across the HEXFET when it is switched OFF (at a later point in the cycle, not shown in Figure 16). This overvoltage, again, must be clamped; unfortunately, the energy dissipated in the clamp at turn-OFF is significantly greater than the energy saved at turn-ON.

For the above reasons, a linear inductor inserted in the circuit to slow down the rate of change of current is not generally attractive, to say nothing of the fact that it is an added "power circuit" component. As a point of interest, however, it is worth noting that a series inductor actually reduces the total energy dissipated in the HEXFET itself, at the expense of extra overall energy dissipation in the clamps and snubbers.

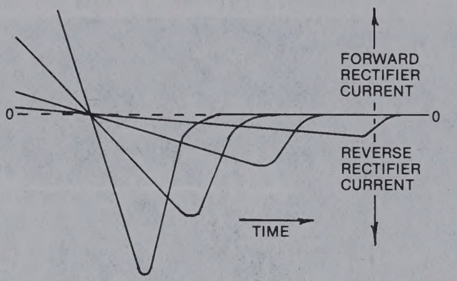
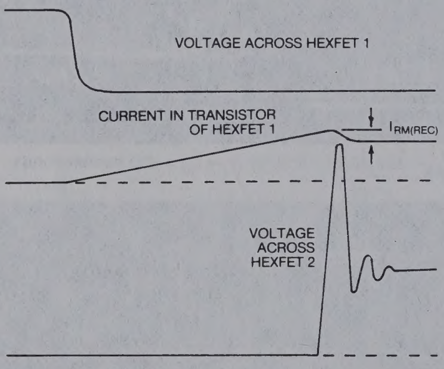
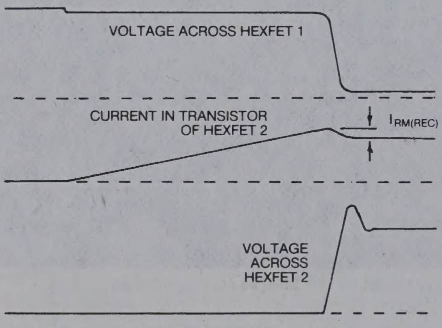


Figure 15. Reducing the Peak Rectifier Reverse Current by Reducing the Rate of Change of Current.



(a) Slowing the Rate of Change of Current by Inserting a Series Inductor



(b) Slowing the Rate of Change of Current by Slowing the Applied Drive Signal

Figure 16. Alternative Circuit Techniques for Controlling the Peak Reverse Recovery Current

The other solution mentioned, which avoids the need for an additional power circuit inductor, is simply to slow down the switching-ON of the HEXFET by appropriately slowing down the rise of the applied gate drive signal. The effect on the circuit operation is illustrated in Figure 16b.

The peak current carried by the HEXFET can be reduced to almost any desired extent, at the expense of prolonging the high dissipation period, and hence increasing the energy dissipation at switch-ON. The practical oscillograms in Figure 14b illustrate this technique. By slowing the total switch-ON time $(t_1 + t_a)$ from 300ns to 1.8μs, the peak current, I_{MAX}, has been decreased from 20A to 10A. The energy dissipation associated with the "unrestrained" switch-ON in Figure 14a is 0.9mJ, whereas it is 2.7mJ for the controlled switch-ON of Figure 14b. Note, however that the average switching losses at a switching frequency of, say, 5kHz, are quite manageable—4.5W and 13.5W for Figures 14a and 14b, respectively.

Note that it is not necessary to slow the switching-OFF of the HEXFET, hence the energy dissipation at switch-OFF will be relatively small by comparison with that at switch-ON. For operation at frequencies up to a few kHz, where ultra fast switching is not mandatory, slowing of the applied gate drive signal to reduce the peak reverse recovery current of the rectifier (of the opposite device) will offer a good practical solution.

Use of External Fast Recovery Rectifier

As will be seen in the next section, for many applications where high switching frequency is required, the reverse recovery characteristic of the integral reverse rectifier is not a factor, even though this rectifier is used to carry inductive load current.

There will, however, be some high-frequency applications which require a reverse rectifier in which reverse recovery will be critically important, and in which the reverse recovery time of the integral reverse rectifier will not be fast enough.

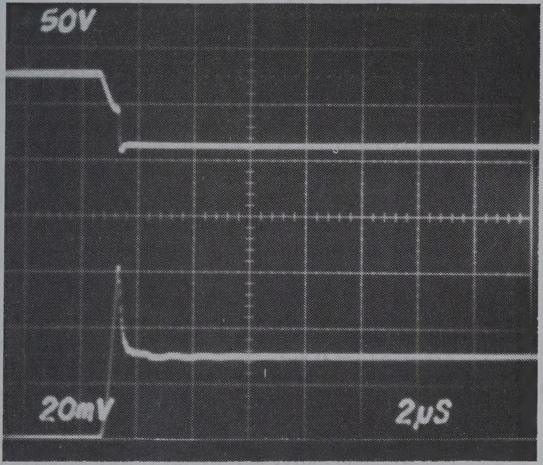
In this event, the first approach is to connect an external fast recovery rectifier, or Schottky rectifier, across the HEXFET. So long as the conduction voltage drop of the external rectifier is appropriately lower than that of the integral rectifier, the external rectifier will carry the builk of the "freewheeling" current, and the reverse recovery characteristic seen in the circuit will be that of the fast external rectifier. An example of the reduction in peak reverse recovery current obtained by connecting an external fast rectifier across the HEXFET is illustrated in Figure 17. With an external rectifier across the IRF130, the peak current at switch-ON is reduced from 25A to 16A, and the switching energy in the HEXFET is reduced from 500 to 120μJ.

This solution will generally be applicable for low voltage HEXFETs, for which compatible low voltage drop fast recovery rectifiers or Schottky rectifiers are commercially available. For high voltage HEXFETs, however, fast recovery rectifiers are not yet generally available with sufficiently low conduction voltage. For these applications, it may be necessary to connect a rectifier or Schottky rectifier in series with the HEXFET, and a separate, high voltage, fast recovery rectifier across the combination. The series rectifier will block reverse current from flowing through the integral reverse rectifier of the HEXFET, thereby alleviating the recovery problem by shifting it to the faster external rectifier.

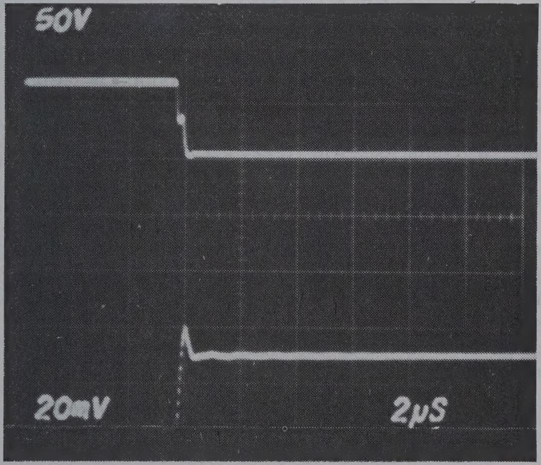
Where Reverse Recovery is Not Critical

All "full wave" voltage-fed inverter circuits use at least one of the tandem-switch circuit modules shown in Figure 12 (or an equivalent derivative thereof). A half bridge circuit, for example, uses one of these modules; a full single-phase bridge circuit uses two, and a three-phase bridge circuit uses three.

As has been seen, reverse recovery presents a difficulty when commutating current from a rectifier to a transistor. Whether or not this operating condition occurs depends upon the operating mode of the circuit. It does *not* occur in an inverter in which each output half cycle comprises a single voltage pulse, so long as the load is resistive or inductive. With a resistive load, the rectifiers do not come into play With an inductive load, current is commutated from a transistor into an opposite rectifier; but never from a rectifier into an opposite transistor (it simply reverses



(a) I_{MAX} = 25A, di/dt = 40A/µs
Switching Energy ≑ 500 µJ



(b) I_{MAX} = 12A, di/dt = 40A/µs
Switching Energy ≑ 120 µJ

Figure 17. Oscillograms of IRF130 Switching into a Current of 12A Freewheeling in (a) The Reverse Rectifier of Another IRF130 and (b) an External Fast Rectifier Connected Directly Across the Reverse Rectifier of an IRF130.

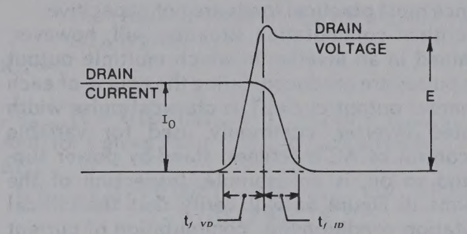
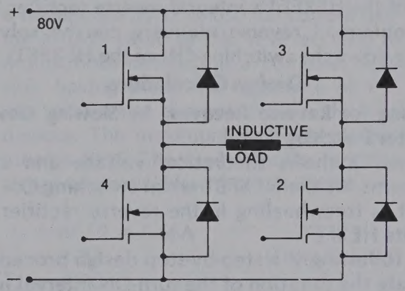
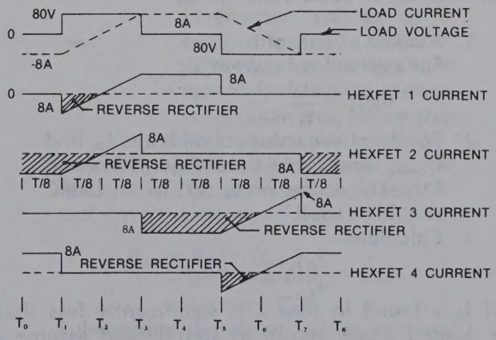


Figure 18. Voltage and Current Waveforms When Switching Output Current I_o from Transistor to Opposite Rectifier



(a) DC to AC Inverter With Inductive Load



(b) Theoretical Operating Waveforms

Figure 19. Inverter Circuit and Waveforms

naturally from the rectifier to the transistor of the *same* device, at an instant determined by the phase angle of the load, not by the inverter switching). Inspection of the waveforms in Figure 6c and Figure 19b will verify this rule. This is an important point, because it means that the reverse rectifier of the HEXFET is not frequency limiting in conventional "single voltage pulse" switching inverter circuits (i.e., most common switching mode power supply circuits), even though these circuits can utilize the rectifier to carry inductive current.

The situation is different with a capacitive load, for which the current leads the voltage. For a capacitive load, the current is instantaneously "negative" in a given switch at the moment of commutation, and current is now commutated from a rectifier to the opposite transistor. But this is of no great practical concern, since most practical loads are not capacitive.

The critical commutation situation will, however, be obtained in an inverter in which multiple output voltage pulses are produced during the course of each fundamental output cycle. The classical pulse width modulated inverter, commonly used for variable speed control of AC machines, stand-by power supplies, and so on, is an example. Inspection of the waveforms in Figure 6c will verify that the critical commutation condition (i.e., commutation of current from a rectifier to an opposite transistor) does indeed occur in this pulse width modulated (PWM) circuit. Fortunately, most practical applications which utilize multi-pulse width modulation techniques operate at a rather modest modulating frequency, usually not above a few kHz. In these applications, use can be made of the HEXFET's integral reverse rectifier, whilst the problem of reverse recovery can be solved by slowing down the switching-ON of the HEXFETs.

Design Calculations

Designing for Reverse Recovery by Slowing Down the Transistor Switching Speed

Figure 13 shows theoretical voltage and current waveforms for the HEXFET when switching-ON into a current I_O freewheeling in the reverse rectifier of an opposite HEXFET.

The following is a step-by-step design procedure to calculate the duration of the turn-ON interval needed to keep the peak current, I_{MAX}, to a desired value. I_{MAX} must not, of course, exceed I_{DM}.

1. Assume a value of t_1
   For a given load current, I_O:
   $$di/dt = \frac{I_O}{t_1}$$
2. For the above values of di/dt and I_O, find $t_{a(max)}$ from Table 1 and Figures 11a and 11b. The value of t_a for T_J = 150°C should be used.
3. Calculate:
   $$I_{MAX} = \frac{I_O}{t_1}(t_{a(max)} + t_1)$$

If I_{MAX} found in step 3 is significantly less than the desired value, return to step 1, and assume a lower value of t_1. If I_{MAX} is higher than the desired value, return to step 1, and assume a higher value of t_1. Repeat until a value of t_1 is found for which I_{MAX} is approximately equal to the desired value.

Example:

The regenerative chopper circuit shown in Figure 4 uses IRF330 HEXFETs. It delivers a smooth full load output current of 3A, and operates from a 300V supply. For the "motoring" mode of operation, the "transistor" of HEXFET 1 and the "rectifier" of HEXFET 2 carry the load current during the ON and OFF intervals of HEXFET 1, respectively. Calculate the required rise time period, t_1, of the current (Figure 13b) to keep the peak current I_{MAX} in the transistor to 7A.

1. Assume $t_1 = 1\mu s$
   then $di/dt = \frac{3}{1} = 3A/\mu s$
2. From Table 1, $t_{a(max)}$ = 470ns for an initial forward rectifier current of 8A, (I_F=1PU) and a di/dt of 100A/μs (di/dt = 1PU). From Figures 11a and 11b, corrected $t_{a(max)}$ for an initial forward current of 3A (0.375PU) and a di/dt of 3A/μs, is given by:
   $$t_{a(max)} = 470 \times 0.73 \times 2.8$$
   $$= 961 \text{ nanoseconds}$$
3. $$I_{MAX} = \frac{3}{1}(0.772 + 1)$$
   $$= \underline{\underline{5.88A}}$$

Reiterating to come closer to I_{MAX} = 7A:

1. Assume $t_1 = 0.8\mu s$
   Then $di/dt = \frac{3}{0.8} = 3.75A/\mu s$
2. $$t_{a(max)} = 470 \times 0.73 \times 2.5$$
   $$= 858 \text{ nanoseconds}$$
3. $$I_{MAX} = \frac{3}{0.8}(0.755 + 1)$$
   $$= \underline{\underline{6.96A}}$$

This is sufficiently close to the desired value of I_{MAX} of 7A. Hence the required value of t_1 is approximately 0.8μs. This can be obtained by appropriately slowing down the ON drive pulse to HEXFET 1. Once t_1 is known, it is then possible to calculate the switching losses in HEXFET 1. This is dealt with in the next section.

Complete Thermal Design

In this section, we show how to make design calculations that take account of the total losses in the HEXFET, due to the conduction in the transistor and the rectifier, as well as the transitional switching losses. These calculations should be made at the design stage to ensure that the HEXFET operates within its rated limits.

The basic design criteria that must be satisfied are:

(a) The peak operating junction temperature must be within the rated 150°C limit.

(b) The RMS drain current must not exceed the rated continuous direct current, I_D.

(c) The peak drain current must not exceed the rated pulsed current, I_{DM}.

The better the heatsinking, the greater will be the permissible total average power dissipation. The total dissipation in general is due to the flow of "transistor" current and "rectifier" current, and switching losses. The total of these three components of power dissipation must be kept within the limits allowed by the cooling arrangement and the ambient temperature.

Of course, as with all semiconductor devices, it is good design practice to maintain a reasonable safety margin between the actual maximum operating values and the rated limits.

The transistor conduction power, P_T, is given approximately by:

$$P_T = I_T^2 R_{D(on)} [1 + 0.007 (\Delta T_{JA} + T_A - 25)] \qquad (1)$$

Where I_T = RMS value of "transistor" current
$R_{D(on)}$ = on resistance at 25°C
T_A = ambient temperature − °C
ΔT_{JA} = temperature rise, junction to ambient

The terms within the brackets [ ] account for the typical 0.7%* increase in $R_{D(on)}$ per degree Centigrade temperature rise above 25°C.

The rectifier conduction power, P_R, is given (conservatively) by:

$$P_R = I_{R(AV)} V_C \qquad (2)$$

Where $I_{R(AV)}$ = average rectifier current
V_C = conduction voltage drop of rectifier at peak rectifier current

The switching energy depends upon the voltage and current being switched, and the type of load. In the context of chopper and inverter circuits that utilize the integral reverse rectifier, in which a load current I_O that stays "constant" during the commutation interval is switched from a "transistor" to an opposite "rectifier" and/or vice versa, the switching energy is approximated by the relationships given in Table 2.

TABLE 2
Approximate Expressions for Switching Energy

Switching Condition	Switching Energy In "Transistor" Joules	Switching Energy In Opposite "Rectifier" Joules
Transistor switching ON into current I_O already flowing in opposite rectifier	$\frac{EI_{max}}{2}(t_1 + t_{a(max)} + t_{b(max)})$ $+ E(1_{max} - I_o)\frac{t_{b(max)}}{3}$ Note 1	$E(I_{MAX} - I_O)\frac{t_{b(max)}}{6}$ Note 1
Transistor switching OFF and transferring current I_O into opposite rectifier	$\frac{EI_O}{2}(t_{f(V_D)} + t_{f(I_D)})$ Note 2	———

Note 1 See waveforms in Figure 13. t_a is found from Table 1 and Figures 11a and 11b. $t_{b(max)}$ can be taken to be 1.2 × the value of $t_{b(min)}$ given in Table 1, multiplied by the appropriate correction factors taken from Figures 11a and 11b.

Note 2 See waveforms in Figure 18. Values of $t_{f(V_D)}$ and $t_{f(I_D)}$ depend upon drive circuit. Typical values for each are 50 to 100 nanoseconds for IR's HEXFETs.

The total switching loss, P_S, is the total switching energy, ε_T, multiplied by the operating frequency, f. ε_T is the sum of the energies due to the individual switchings that take place in each fundamental operating cycle.

$$P_S = \varepsilon_T \cdot f$$

The total power dissipation in a given HEXFET is the sum of the transistor and rectifier conduction powers, P_T and P_R, respectively, and the total switching power, P_S.

$$P = P_T + P_R + P_S$$
$$= I_T^2 R_{D(on)} [1 + 0.007 (\Delta T_{JA} + T_A - 25)] + I_{R(AV)} V_C + P_S \qquad (3)$$

Since:

$$\Delta T_{JA} = P R_{JA}$$

Where R_{JA} = junction to ambient thermal retance

The required value of R_{JA} for a given value of ΔT_{JA} is given by:

$$R_{JA} = \frac{\Delta T_{JA}}{I_T^2 R_{D(on)} [1 + 0.007 (\Delta T_{JA} + T_A - 25)] + I_{R(AV)} V_C + P_S} \qquad (4)$$

And, for a given value of R_{JA}, ΔT_{JA} is given by:

$$\Delta T_{JA} = \frac{I_T^2 R_{D(on)} R_{JA}[1 + 0.007(T_A - 25)] + I_{R(AV)} V_C R_{JA} + P_S R_{JA}}{1 - 0.007\, I_T^2 R_{D(on)} R_{JA}} \qquad (5)$$

Design Examples

The following specific examples illustrate the generalized design procedures given.

1. In the AC switch circuit shown in Figure 5, it is required to use two IRF350s to switch a continuous 60Hz sinusoidal current having a RMS value of 8A. It is required to mount both devices on a common heatsink, having a thermal resistance of 1°C per total watts dissipated from the two devices. The maximum ambient temperature is 40°C. Check whether the junction temperature will be within safe limits.

   $I_T = 8/\sqrt{2} = 5.66\text{A}$
   $R_{D(on)} = 0.3\Omega$ (From Table 1)
   $T_A = 40°\text{C}$
   $I_{R(AV)} = \sqrt{2}.8/\pi = 3.6\text{A}$
   $V_C = 0.1\text{V}$ (From Figure 7b. This is the conduction voltage at a peak current of 11A, at T = 25°C. The conduction voltage at higher temperature is less than this; hence this is a conservative number).

   The effective thermal resistance of the heatsink is 2°C per watt dissipated in *each* device. Hence:

   $$R_{JA} = R_{JC} + R_{CS} + 2$$
   $$= 0.83 + 0.4 + 2$$
   $$= 3.23 \text{ deg. C/W}$$

   Substituting the above values in equation (5) above, and neglecting switching losses which will be negligible in this application at this operating frequency, gives: $\Delta T_{JA} \doteq \underline{58.5°C}$

---

*The actual temperature coefficient depends upon the specified device type, and can vary from 0.45 to 0.85%. The figure used of 0.7% is a typical value; reference can be made to the individual device data sheet where greater accuracy is necessary.

Hence $T_J = 58.5 + 40$

$= \underline{98.5°C}$

This is well within the rated $T_{J(max)}$ of 150°C.

2. The bridge inverter circuit using IRF130 HEXFETs shown in Figure 19a operates at 100kHz. Waveforms of current through the individual devices are shown in Figure 19b. For this "single voltage pulse" operating mode, current always commutates from a transistor into a rectifier, and never from a rectifier into a transistor. Rectifier reverse recovery is not therefore a factor, and switching times $t_{f(VD)}$ and $t_{f(ID)}$ (see Figure 18) are 70 nanoseconds each.

   Calculate the thermal resistance of the device heatsink required to keep the junction temperature of HEXFETs 1 and 4 to 125°C, and the junction temperature of HEXFETs 2 and 3 (which do not work so hard) if mounted on similar heatsinks. The maximum ambient temperature is 40°C. $R_{D(on)}$ is 0.18 Ohm, T_A is 40°C, and V_C can be taken to be 1.15V.

Transistor and Rectifier Conduction Losses:

HEXFETs 1 and 4: $I_T = \sqrt{\frac{8^2}{3^2}\cdot\frac{1}{8} + 8^2\cdot\frac{1}{4}}$

$= \underline{4.11A}$

$I_{R(AV)} = \frac{8}{2}\cdot\frac{1}{8}$

$= \underline{0.5A}$

Hence from (1):

$P_T = 4.11^2 \cdot 0.18[1 + .007\,(85 + 40 - 25)]$

$= \underline{6.2W}$

$P_R = 0.5 \cdot 1.15$

$= \underline{0.575W}$

HEXFETs 2 and 3: $I_T = \frac{8}{3}\sqrt{\frac{1}{8}}$

$= \underline{0.943A}$

$I_{R(AV)} = \frac{8}{2}\cdot\frac{1}{8} + 8\cdot\frac{1}{4}$

$= \underline{2.5A}$

Hence P_T

$= 0.943^2 \cdot 0.18[1 + .007\,(\Delta T_{JA} + 40 - 25)]$

$= 0.16\,[1 + .007\,(\Delta T_{JA} + 15)]$ W

$P_R = 2.5 \cdot 1.15$

$= \underline{2.875W}$

Switching Losses:

HEXFETs 1 and 4 (HEXFET 1 taken as example. Refer to Figure 19.)

At T_1, current is switched into HEXFET 1 rectifier from Hexfet 4. From Table 2:

$\varepsilon \doteq 0$

At T_5, current is switched from HEXFET 1 into rectifier of HEXFET 4. From Table 2:

$\varepsilon = \frac{80.8}{2}(70 + 70) \cdot 10^{-9}$J

$= 0.0448 \cdot 10^{-3}$J

$\therefore P_S = 0.0448 \cdot 100$

$= \underline{4.48W}$

HEXFETs 2 and 3: By similar analysis:

$\varepsilon = 0.0448 \cdot 10^{-3}$J

And $P_S = \underline{4.48W}$

Required heatsink thermal resistance for HEXFETs 1 and 4:

Substituting the appropriate values into equation (4) gives:

$R_{JA} = \frac{125 - 40}{6.2 + 0.575 + 4.48}$

$= \underline{7.55}$ deg. C/W

$R_{J\text{-}S} = 1.67\,(J-C) + 0.4\,(C-S)$

$= 2.07$ deg. C/W

$\therefore R_{SA} = 7.55 - 2.07$

$= \underline{5.48}$ deg.C/W

This is the solution to question (a).

Substituting the appropriate values for HEXFETs 2 and 3 into equation (5) and using $R_{JA} = 7.51$ deg.C/W gives:

$$\Delta T_{JA} = \frac{0.943^2 \cdot 0.18 \cdot 7.55[1 + 0.007 \cdot 15] + 2.5 \cdot 1.15 \cdot 7.55 + 4.48 \cdot 7.55}{1 - 0.007 \cdot 0.943^2 \cdot 0.18 \cdot 7.55}$$

$= 56$ deg.C

$\therefore T_J = \underline{96.2°C}$

This is the solution to (b).

3. The regenerative chopper circuit using IRF330 HEXFETs shown in Figure 4a delivers a full load output current of 3A, and operates from a supply voltage of 300V. For the "motoring" mode of operation, the transistor of HEXFET 1 and the rectifier of HEXFET 2 carry the load current during the ON and OFF intervals of HEXFET 1, respectively. The rise time period, t_1 (Figure 13), of the current is purposefully slowed down to 0.8μs. The corresponding value of I_{MAX} is 7A and $t_{a(max)} = 858$ nanoseconds, as calculated in the previous section headed "Designing for Reverse Recovery by Slowing Down the Transistor Switching Speed."

$t_{f(VD)}$ and $t_{f(ID)}$ (Figure 18) are each 100 nanoseconds. The operating frequency is 5kHz. Calculate the conduction and switching losses in HEXFET 1, for a maximum conduction duty cycle of 96%. The maximum junction operating temperature is 130°C, and the ambient temperature is 45°C. Also calculate the required thermal resistance of the heatsink for HEXFET 1. $R_{D(on)}$ is 1.0 Ohm.

Conduction loss in HEXFET 1:

$= 0.96 \cdot 3^2 \cdot 1.0\,[1 + .007\,(130 - 25)]$

$= 15$W

From Table 1, $t_{b(min)}$ for $I_F = 8$A, di/dt = 100A/μs, and $T_J = 150°C$, is 95 nanoseconds.

From Figures 11a and 11b, corrected value of $t_{b(min)}$ for an initial forward current of 3A (0.375PU) and a di/dt of 3.75A/μs is given by:

$t_{b(min)} = 95 \times 0.82 \times 5.1$

$= 397$ nanoseconds

$\therefore t_{b(max)} = 397 \times 1.2 = 476$ nanoseconds (See Note 1 to Table 2).

And, from Table 2:

Switching Energy

$= \frac{300 \cdot 7}{2}(0.8 + 0.858 + 0.476) + 300\,(7 - 3)\frac{0.476}{3}$

$$+ \frac{300.3}{2}(0.1+0.1)$$

$$= 2.52\text{mJ}$$

$$\therefore \text{Switching losses at 5kHz} = 2.52 \times 5$$

$$= \underline{\underline{12.6\text{W}}}$$

$$\text{And total power dissipated} = 15 + 12.6$$

$$= \underline{\underline{27.6\text{W}}}$$

R_{JS} for IRF330 is 1.67 (J − C) + 0.4 (C − S) = $\underline{\underline{2.07}}$ deg. C/W

$$\text{Therefore } T_c = 130 - (2.07 \cdot 27.6)$$

$$= 73°\text{C}$$

Hence temperature rise from heatsink to ambient

$$= 73 - 45$$

$$= 28 \text{ deg.C/W}$$

And required thermal resistance of heatsink

$$= \frac{28}{25.4}$$

$$= 1.1 \text{ deg.C/W}$$

Conclusions

The HEXFETs integral reverse rectifier, far from being a "parasitic" component, can be utilized in its own right, and indeed has a current rating equal to that of the transistor. This article has shown where and how to use this rectifier, what cautions should be observed, and where it cannot be used.

Generally, the HEXFET's integral reverse rectifier will be applicable in the following areas:

(a) DC to AC inverters, which operate with one voltage pulse per output half cycle. In these circuits, the use of the integral reverse rectifier does not limit the switching frequency, so long as the load is inductive (as it normally is).

(b) Multi-pulse (PWM) DC to AC inverters, such as those used for variable frequency speed control of AC machines, and general purpose AC power supplies. Rectifier switching speed will usually restrict operating frequency to the 5-10 kHz range, but in many cases this will not be practically limiting.

(c) DC to DC choppers, such as are used in regenerative DC motor controllers. Again, rectifier switching speed will usually limit switching frequency to the 5-10kHz range.

(d) Bidirectional AC switching circuits.

The HEXFET's integral reverse rectifier has so far been largely overlooked. Circuit designers can now take serious note of it; it represents yet another potential application advantage of IR's HEXFETs. ☐

This application note was co-authored by the following technical staff members of International Rectifier's Application Engineering Department: Brian R. Pelly, Bill Fragale and Brian Smith.

CHAPTER 6

APPLICATION NOTE 933

Switching transients in high-frequency, high-power converters using power MOSFETs

Abstract

The use of metal-oxide-semiconductor field-effect transistors in dc-to-dc converters as the controlled switch has become practical with the development of power MOSFETs. The use of these devices in parallel in a high-frequency, high-voltage, high-power converter is investigated. Stray circuit inductances in a two-winding voltage-or-current step-up converter have a pronounced effect on some of the currents and voltages during the turning-on and turning-off intervals.

Introduction

With the advent of the power metal-oxide-semiconductor field-effect transistor (MOSFET), another realistic choice is available for the power switch in high-power, high-frequency, high-voltage, dc-to-dc converters. When compared to the bipolar junction transistor (BJT), the MOSFET offers advantages of no second breakdown, lower switching losses, and simplicity of drive circuitry, while having the disadvantage of a relatively high resistance during the ON state. The use of MOSFETs in parallel to reduce the ON-state resistance and to increase the power handling capabilities of a converter is an effective design procedure, although paralleling MOSFETs in a switching application is not without certain perils. The effects of stray circuit inductances in a converter using one or more MOSFET switches are important during the turning-on and turning-off intervals, especially at high switching frequencies when the total period of the power conversion cycle is only a few microseconds in duration.

The converter configuration investigated in this research is the constant-frequency, two-winding, voltage-or-current step-up energy-storage circuit. This paper addresses some of the phenomena associated with paralleling of MOSFETs and studies the impact on circuit performance of stray circuit inductances in a dc-to-dc converter. Circuit models which lead to a quantitative analysis and to a computer simulation study of circuit parameter variations are presented.

Overview

The focus for the study of the behavior of MOSFETs in power handling circuits in this paper is the two-winding voltage-or-current step-up converter, sometimes referred to as the buck-boost configuration. Research has been directed toward the development of a converter for eventual application in a high-voltage, high-power, high-frequency space application. Some future space applications will require power at the level of tens of kilowatts. One approach to the management of power within a large spacecraft system calls for distribution of electrical energy at relatively high dc voltages in order to save on conductor weight. To further reduce the weight of the system, a switching frequency considerably higher than conventionally used in converters is desirable. A number of potential problems arise along with the advantages of a high-voltage, high-frequency system. The frequency-related problems include increased losses in various components, such as: (1) the power switch and commutating diode during the turning-on and turning-off intervals; (2) the magnetic core material and windings, and (3) the filter capacitors. Stray circuit and transformer inductances which have a significant effect on switching times must be taken into account in the analysis of loss mechanisms in the power switch and diode. The use of higher voltage levels leads to potential problems in voltage breakdown of the power switch and diode and of the input and output capacitors.

A two-winding voltage-or-current step-up converter using two MOSFETs in parallel as the power switch is shown in Figure 1. One version of the circuit was operated with a constant switching frequency of 100 kHz and a nominal output power of 400W. The two MOSFETs Q1 and Q2 are driven into the conducting state from a voltage drive circuit with separate resistors R_{G1} and R_{G2} in series with the two gates. These separate gate resistors act as loss elements to increase the dissipation in potential parasitic resonant circuits in the gate and drain leads which can be responsible for very high frequency oscillations in a parallel configuration of active devices.

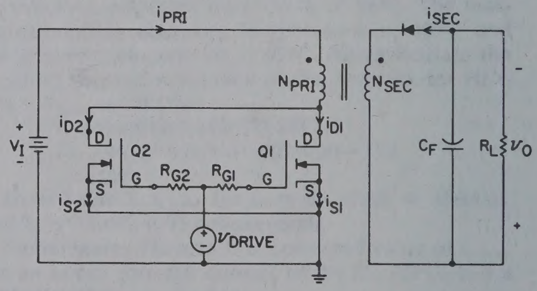


Figure 1. Two-winding voltage-or-current step-up converter with two parallel MOSFETs.

As a further orientation to the particular configuration

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under discussion, waveforms of important currents and voltages for a complete switching cycle of the two-winding converter are shown in Figure 2(a), along with the output of a computer simulation program for the same circuit variables in Figure 2(b). The waveforms are analogous to those normally seen in a circuit using a BJT switch except that the MOSFET gate-to-source voltage is shown in place of base current. The computer simulation waveforms are for a set of reference conditions which are comparable to, but not identical to, those of the experimental converter.

The discussion of a complete switching cycle begins with the turning-on portion of the waveforms. During this time interval, the MOSFET switch is driven from its *off* or below-threshold state through an *active* or constant-current region into an *on* or ohmic state. Using a pulse generator with fast risetime for v_{DRIVE} to drive the gates of the MOSFETs, the gate-to-source voltages v_{GS1} and v_{GS2} rise quickly toward a target voltage corresponding to the applied gate-drive pulse level, then undergo a sharp break in slope as the MOSFETs are driven into the active state. For obtaining the experimental waveforms, the MOSFETs have been chosen with closely matched threshold voltages V_T. The sharp break in the slope of the gate-to-source voltage occurs as the MOSFETs are driven into the active region and a feedback voltage appears across a small, but yet finite, stray inductance in the source lead of the switches which acts to counteract the effect of the gate drive voltage. This negative feedback effect during the turning-on interval increases the time required to pass from the threshold condition through the active region into the ohmic region as the time rate of change of the drain currents is lowered by the reduction in the gate-to-source voltage. An important consequence of this reduced rate-of-rise of drain current is that the drain-to-source voltage does not fall directly to the low value eventually obtained when the ohmic region is entered. Instead, a small plateau-like region may be observed in the drain-to-source voltage which is terminated as the ohmic region is entered. This "plateau", which is due principally to L(di/dt) voltage drops across small stray circuit inductances — principally in the drain circuit — has a direct effect on the power dissipated by the switches during the turning-on interval. Another feature to note is that during this time, the secondary-circuit diode is still in a conducting state. During the initial part of the turning-on interval, diode current is flowing in the forward direction, but decreasing in amplitude as the MOSFET switches pick up the current to maintain an essentially constant mmf in the magnetic core. In the latter portion of the interval, the diode is still forward-biased, but its current is now negative. As a direct result of this reverse-recovery effect, the total drain current overshoots the value required to maintain constant mmf under perfect commutation, thus causing additional power to be dissipated during this portion of the switching intervals. Similar effects also appear in converters using BJT switches [1-3].

Continuing with a qualitative discussion of the complete switching cycle, as the gate-to-source voltage continues to increase, the MOSFET switches are driven beyond the active region into the ohmic region, and the drain-to-source voltage falls rapidly to a value determined by the drain currents and the drain-to-source ON resistances. Additional energy is stored in the magnetic core as the primary current increases in an essentially

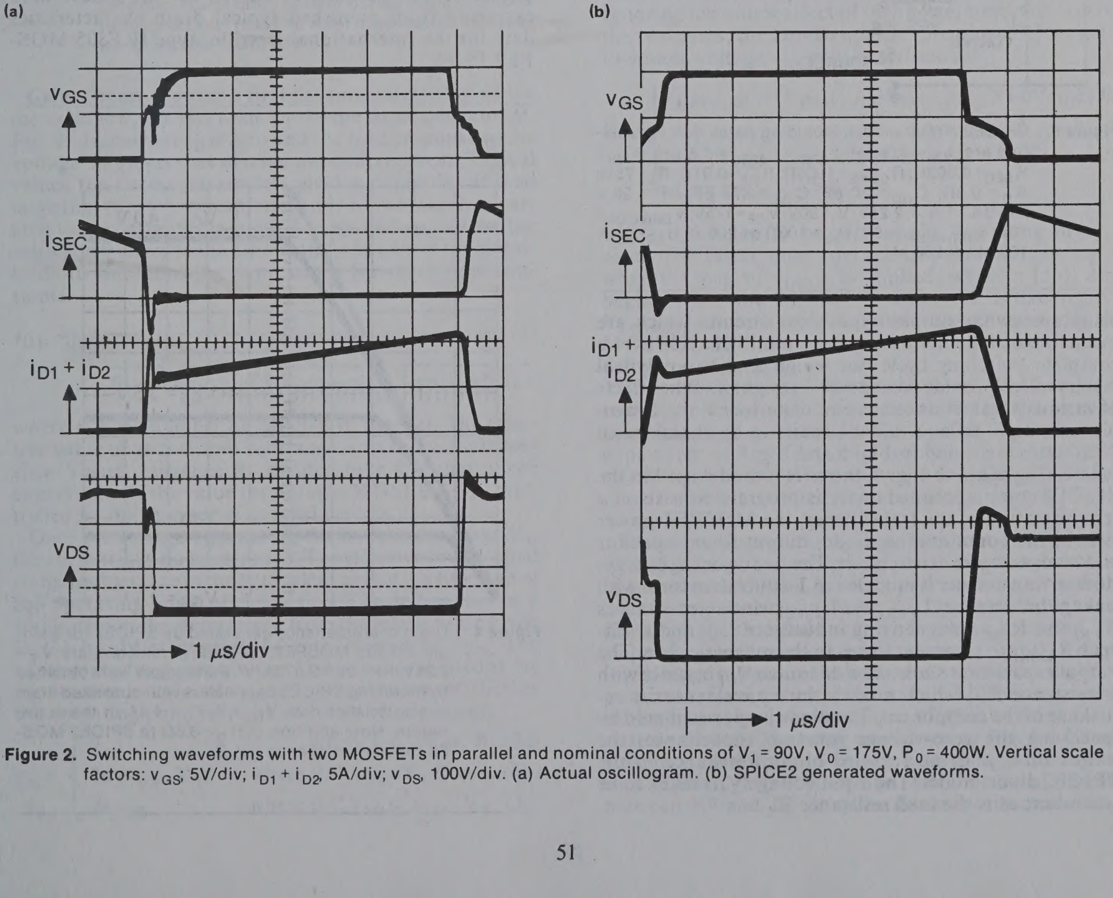

Figure 2. Switching waveforms with two MOSFETs in parallel and nominal conditions of $V_1 = 90V$, $V_0 = 175V$, $P_0 = 400W$. Vertical scale factors: v_{GS}; 5V/div; $i_{D1} + i_{D2}$, 5A/div; v_{DS}, 100V/div. (a) Actual oscillogram. (b) SPICE2 generated waveforms.

linear manner during the on-time of the switches at a rate determined by the value of the input voltage and the primary inductance.

Modeling and Analysis of the Converter Circuit

To adequately analyze the converter circuit in Fig. 1, several levels of modeling and analysis complexity are required. In order to obtain a realistic portrayal of the time-domain behavior of the significant currents and voltages in the converter circuit, computer-aided analysis is employed using the circuit analysis program SPICE2 [4]. To obtain realistic waveforms that match reasonably well those which are experimentally observed requires a reasonably complex model, since the nonlinear characteristics of the power switch and commutating diode are critical elements in the circuit. The equivalent circuit in Fig. 3 is used to represent the converter circuit for the computer-aided analysis. Other analyses are performed using somewhat simpler equivalent circuits which are incapable of fully describing the circuit behavior over a complete switching cycle but which lead to analytical results which provide considerable insight into the effects of various parameters on the circuit performance. Examples of simplified equivalent circuits to be examined in detail later are found in Fig. 5 and Fig. 8

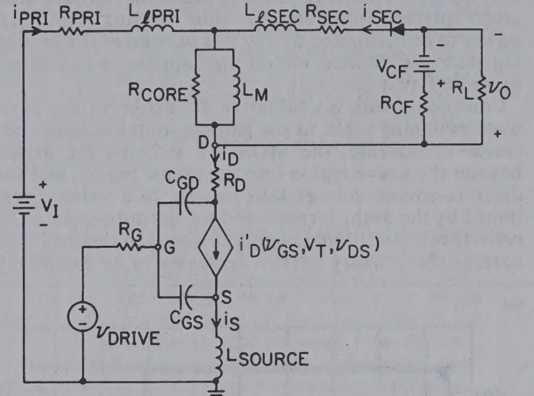

Figure 3. SPICE2 circuit model, including parasitics. Parameters are: $L_M = 115\ \mu H$; $L_{\ell PRI} = L_{\ell SEC} = 1.5\ \mu H$; $R_{PRI} = R_{SEC} = 0.003\Omega$; $R_{CORE} = 1000\Omega$; $R_{CF} = 0.01\Omega$; $R_L = 75\Omega$; $R_D = 0.8\Omega$; $C_{GD} = 30$ pF; $C_{GS} = 770$ pF; KP = 2k = 2.873A/V²; $V_T = 2.25V$; $V_I = 90V$; $V_{CF} = 175V$; $V_{DRIVE,ON} = 10V$; $V_{DRIVE,OFF} = 0V$; $R_G = 100\Omega$ or $200\ \Omega$; $L_{SOURCE} = 100$ nH or 200 nH.

Referring again to Fig. 3, the circuit model used in the SPICE2 computer-aided analysis program consists of a representation of the transformer, the MOSFET power switch, the commutating diode, output filter capacitor and load, and gate drive circuit. The two-winding energy-storage transformer is modeled in T-equivalent form with leakage inductances $L_{\ell PRI}$ and $L_{\ell SEC}$, winding resistances R_{PRI} and R_{SEC}, magnetizing inductance L_M, and resistance R_{CORE} to represent losses in the magnetic core. The output capacitor is shown as a dc source V_{CF} in series with a resistance R_{CF} which models the equivalent series resistance of the component. The diode is approximated by specifying the zero-voltage junction capacitance, the transit time, and the forward ohmic resistance in the SPICE2 diode model. The input voltage V_I is taken to be a constant as is the load resistance R_L.

For simplicity in the equivalent circuit model, the MOSFET portion of the circuit in Fig. 3 is represented by a single device. The model employed in SPICE2 is the built-in MOSFET set of equations given in Eq. (1).

$$i'_D = \begin{cases} 0 & \text{(below threshold (1a)} \\ & \text{where } v_{GS} - V_T < 0) \\ k\,(v_{GS} - V_T)^2 & \text{(active (1b)} \\ & \text{where } 0 < v_{GS} - V_T < v_{DS}) \\ k v_{DS}[2\,(v_{GS} - V_T) - v_{DS}] & \text{(ohmic (1c)} \\ & \text{where } 0 < v_{DS} < v_{GS} - V_T) \end{cases}$$

These equations describe rather accurately MOSFET behavior in a conventional device with long lateral channel. Power MOSFET characteristics depart somewhat from the square-law dependence between drain current and gate-to-source voltage predicted by (1), particularly in the higher current ranges. Since an adequate model for power MOSFETs has not been devised at this time, the relationships in (1) are used as the basis for analytically establishing parameters such as transconductance and the gate-to-source voltage at which a MOSFET enters the ohmic region for a given drain current. In the equivalent circuit in Fig. 3, only the dc MOSFET model is used, and this is modified by including a resistance R_D to correspond to the estimated value of ON resistance obtained from the manufacturer's data sheet for the MOSFETs used. Since the internal capacitances in the MOSFET model are set to zero, two external fixed capacitances C_{GS} and C_{GD} are used to approximate the device electrode capacitances. A plot of the drain characteristics obtained using the computer model is shown in Figure 4. The parameters chosen for the model were extracted from published typical drain characteristics data for the International Rectifier type IRF305 MOSFET [5, 6].

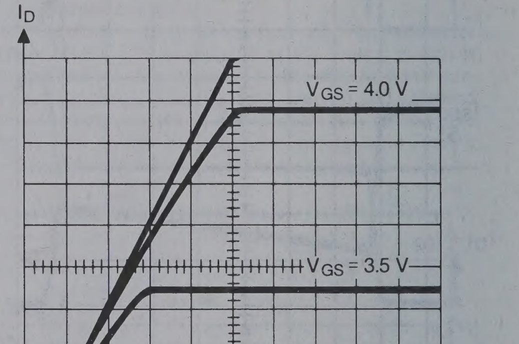

Figure 4. Drain characteristics generated by SPICE2 for a single IRF305 MOSFET; SPICE2 parameters are $V_T = 2.25V$, KP = 2k = 2.873A/V². Parameters were obtained by matching SPICE2 parameters with published drain characteristics data $V_{GS} = 4$, $I_D = 4.4A$ in the active region. Note addition of $R_D = 0.8\Omega$ to SPICE2 MOSFET model, as seen in Fig. 3.

Turning-On Interval

The turning-on interval is defined as the interval between the application of the gate-drive voltage v_{DRIVE} and the entry of the MOSFETs into the ohmic region. The analysis assumes that the drive voltage v_{DRIVE} starts at a level $V_{DRIVE,\ OFF}$ instantaneously rises to its maximum value $V_{DRIVE,\ ON}$. Initially, the gate-to-source voltage v_{GS} is $V_{DRIVE,\ OFF}$ and the gate-to-drain voltage v_{GD} is the negative of the voltage at the drain with respect to ground plus $V_{DRIVE,\ OFF}$. The current i_S in the source inductance L_{SOURCE} is also zero at this initial time. If the current which flows through the gate-to-drain capacitance C_{GD} during the turning-on interval is considered to be very much less than that through the gate-to-source capacitance C_{GS} because of the much larger value of C_{GS}, the equivalent circuit in Figure 5 may be used for an approximate analysis of the response of the gate circuit.

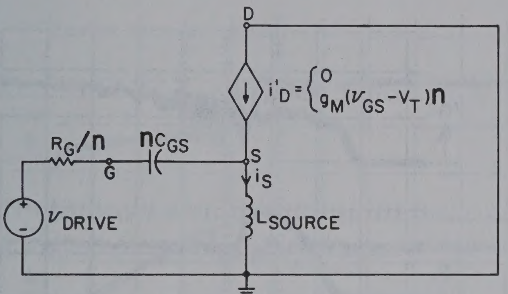

Figure 5. Equivalent circuit for piecewise-linear analysis of gate circuit and drain current during turning-on and turning-off intervals. The letter n represents the number of parallel MOSFETs.

Gate Circuit. Consider first the time interval in which the voltage v_{GS} is less than V_T. In the equivalent circuit, Fig. 5, the current i'_D is zero and the time response to the voltage V_{DRIVE} is that of a second-order system. Typical values for circuit parameters yield a damping ratio so large that the system response is due to two widely separated time constants designated as $\tau 0_1$ and $\tau 0_2$, where the subscript 0 refers to the OFF state. Analysis of the circuit leads to the following expressions for these time constants:

$$\tau 0_1, \tau 0_2 = \frac{2}{\dfrac{R_G}{nL_{SOURCE}} \pm \sqrt{\left(\dfrac{R_G}{nL_{SOURCE}}\right)^2 - \dfrac{4}{L_{SOURCE}nC_{GS}}}} \tag{2}$$

where n is the number of switches in parallel. The effective value of gate-circuit resistance is an individual transistor's gate resistance R_G divided by n and that of the capacitance is the value for a single MOSFET C_{GS} multiplied by the number of parallel devices.

Once the voltage v_{GS} exceeds the threshold voltage V_T, the current i'_D is no longer zero. The effective small-signal transconductance in the equivalent circuit is a function of the operating point of the MOSFETs and of n. For a single device, it is determined from the relationship given in (1) by differentiating i'_D with respect to v_{GS}. The expressions for g_m are given in (3) and are evaluated at the instantaneous value of v_{GS} or v_{DS}, depending on whether the operating point is in the active or ohmic region.

$$g_m = \begin{cases} 0 & \text{where } v_{GS} - V_T < 0 \quad (3a) \\ 2k\,(v_{GS} - V_T) & \text{where } 0 < v_{GS} - V_T < v_{DS} \quad (3b) \\ 2kv_{DS} & \text{where } 0 < v_{DS} < v_{DS} - V_T \quad (3c) \end{cases}$$

In examining the expression for g_m, it can be seen that the transconductance can vary over a considerable range, starting from a value of zero as the active region is entered from the threshold region, increasing to a maximum at the point where the transition is made from the active to the ohmic region, then decreasing to a very small value in the ohmic state.

Analysis of the linear equivalent circuit in Fig. 5 for the condition when i'_D is not zero leads to a new expression for the system time constants which are identified as τ_{A1} and τ_{A2}, where A refers to the active region when entered from the below-threshold condition.

$$\tau_{A1}, \tau_{A2} = 2 \div \left[\frac{R_G}{nL_{SOURCE}} + \frac{g_m}{C_{gs}} \pm \sqrt{\left(\frac{R_G}{nL_{SOURCE}} + \frac{g_m}{C_{gs}}\right)^2 - \frac{4}{L_{SOURCE}\,nC_{GS}}}\right] \tag{4}$$

As before, the values of the gate circuit resistance and capacitance are modified by the factor n when paralleling occurs.

Using reasonable values for the parameters above which correspond roughly to values in the experimental circuit, calculation of the time constants shows that in both cases, before and after passing through the threshold, each equivalent circuit has a dominant time constant. For example, for the case where v_{GS} is less than V_T, with two MOSFETs Q_1 and Q_2 with R_{G1} and $R_{G2} = 100\Omega$, C_{GS1} and $C_{GS2} = 770$ pF and $L_{SOURCE} = 200$ nH, the time constant have values $\tau 0_1 = 4.2$ ns and $\tau 0_2 = 73$ ns. In the edge of the active region, using a value of $g_m = 2k = 2.873$ S obtained from (3) which corresponds to $v_{GS} - V_T = 1$V, the values of τ_{A1} and τ_{A2} are 0.25 ns and 1200 ns, respectively. Ignoring the minor effect of the shorter time constant for the two cases, the approximate expressions for the gate-to-source voltage v_{GS} may be written as:

$$V_{GS} = \begin{cases} V_{DRIVE,OFF} + (V_{DRIVE,ON} - V_{DRIVE,OFF})(1 - e^{t/\tau 0_2}) & (5a) \\ \qquad \text{where } v_{GS} - V_T < 0 & \\ V_T + (V_{DRIVE,ON} - V_T)\,(1 - e^{-t/\tau_{A2}}) & (5b) \\ \text{where } v_{GS} - V_T > 0 & \end{cases}$$

where t is taken to be zero at the beginning of each piece-wise linear time interval, i.e., time in (5a) begins when the step of v_{DRIVE} is applied, while in (5b), time begins when the MOSFETs enter the active region. $V_{DRIVE,OFF}$ is the level of the gate-drive voltage during the MOSFET off-time, while the level during on-time is defined as $V_{DRIVE,ON}$.

Computer-generated waveforms which illustrate these two distinct dominant time constants in the gate-to-source voltage are seen in Fig. 6. This is a ten-times expansion of the first microsecond of the complete switching cycle waveform shown in Fig. (2b). The circuit model which generated these results is that of Fig. 3 where n = 2.

The initial slope of the v_{GS} waveform obtained from the SPICE2 output corresponds to a time constant of approximately 100 ns. This compares rather well with the linear equivalent circuit value of 73 ns calculated using (2). Once the threshold voltage has been exceeded, the slope of v_{GS} with respect to time changes abruptly with an initial slope following the break measured from the computer waveform to be approximately 1100 ns, compared to the linear circuit computation of 1200 ns using (4).

Drain Circuit. The other waveforms in Fig. 6 are drain current i'_D and drain-to-source voltage v_{DS}. During the time of the high rate of change of drain current (usually between 10^7 and 10^8 A/s) the diode is still conducting.

Only after the diode recovers does the very high rate of change drop to a value low enough to reduce the feedback voltage across L_{SOURCE} and drive the MOSFETs into the ohmic region. Expanded time scale waveforms of v_{GS}, i_D and v_{DS} for the experimental converter circuit are pictured in Fig. 7. While the conditions in the experimental circuit and the parameters in the computer simulation have not been matched in detail, the presence of two time constants in the gate-to-source voltage are observed, and the plateau effect in v_{DS} is seen.

The most important result of this feedback due to the source lead inductance is the delay in allowing the drain-to-source voltage to drop to the desired low voltage during the time that the switch is fully ON. This delay is a time of high-power loss in the switch; its duration and the level of the plateau both are influenced in a complex manner by the parameters R_G, C_{GS}, L_{SOURCE} and g_m. The expression in (4) for the linearized gate circuit of Fig. 5 gives an approximation for the time constant of the v_{GS} waveform between the level V_T and the level just prior to entering the ohmic region. With reference to Fig. 8, which will be described more fully later, during this very short turning-on interval, the mmf of the magnetic core does not change, and this effect may be represented by the constant-current generator I_{LM}. Thus, the boundary level for v_{GS} between the active and ohmic regions may be determined by using (1b), letting i_D take on the peak value of diode current at the end of the diode reverse recovery interval, and solving for v_{GS}. Using the subscript A to correspond to this condition and rearranging (1b),

$$V_{DS,A} = \sqrt{\frac{I_{D,A}}{nk}} + V_T \qquad (6)$$

Since the time constant τ_{A2} is relatively long compared to the plateau duration, the slope may be considered constant to a first-order approximation, and this time duration may be obtained from the relationship:

$$t_{PLATEAU} = \tau_{A2}\left[\frac{V_{GS,A} - V_T}{V_{DRIVE,ON} - V_T}\right] \qquad (7)$$

By adding to the elementary gate-circuit model of Fig. 5 equivalent circuit models for the transformer and the input and output circuits, equations may be developed to obtain rough estimates of the plateau level of v_{DS} during turning-on. Figure 8 contains the essential elements for such an analysis. Since during the very short transition for the MOSFETs from ON to OFF and OFF to ON states the mmf of the core essentially is conserved, the magnetizing inductance may be replaced with a constant-current generator indicated by source I_{LM}. This equivalent replacement for the magnetizing inductance L_M has the value of the reflected secondary current at the begin-

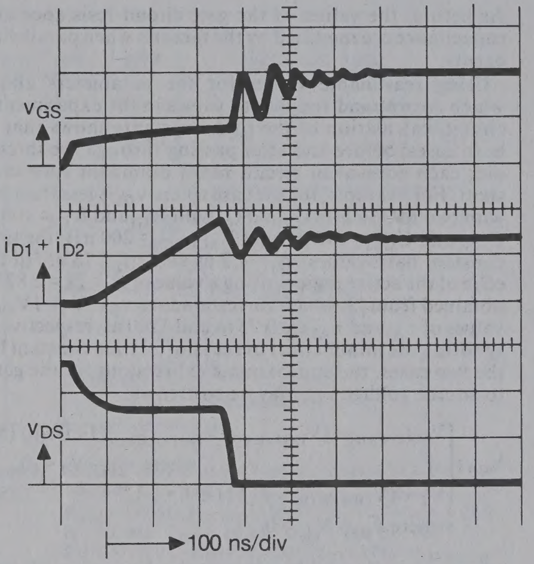

Figure 6. SPICE2 generated waveforms for turning-on interval as expanded from Fig. 2. Vertical scale factors same as Fig. 2.

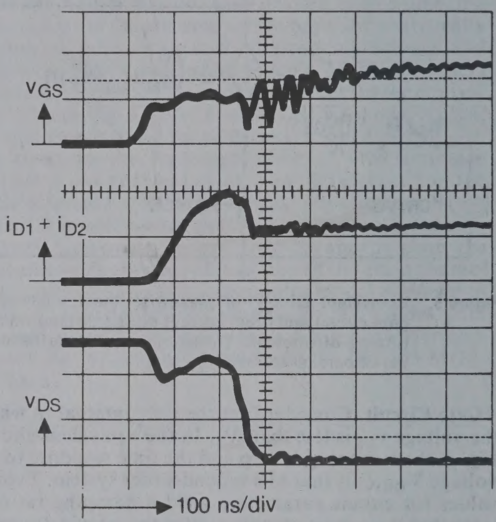

Figure 7. Oscillogram of turning-on interval. Vertical scale factors same as Fig. 2.

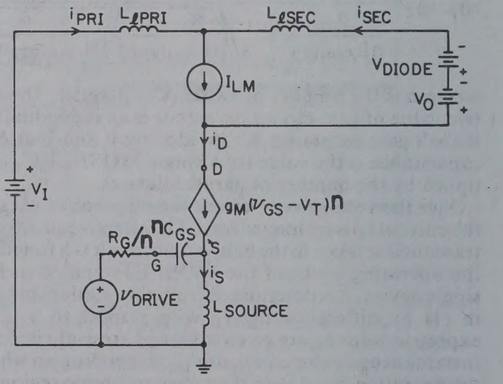

Figure 8. Simplified circuit model for piecewise linear analysis of drain-to-source voltage during turning-on and turning-off intervals.

Only after the diode recovers does the very high rate of change drop to a value low enough to reduce the feedback voltage across L_{SOURCE} and drive the MOSFETs into the ohmic region. Expanded time scale waveforms of v_{GS}, i_D and v_{DS} for the experimental converter circuit are pictured in Fig. 7. While the conditions in the experimental circuit and the parameters in the computer simulation have not been matched in detail, the presence of two time constants in the gate-to-source voltage are observed, and the plateau effect in v_{DS} is seen.

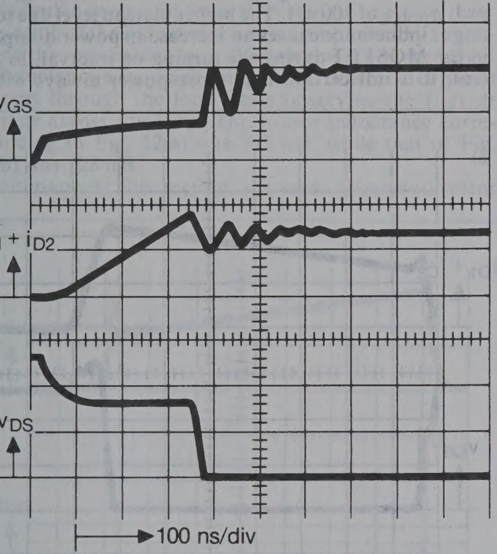

Figure 6. SPICE2 generated waveforms for turning-on interval as expanded from Fig. 2. Vertical scale factors same as Fig. 2.

The most important result of this feedback due to the source lead inductance is the delay in allowing the drain-to-source voltage to drop to the desired low voltage during the time that the switch is fully ON. This delay is a time of high-power loss in the switch; its duration and the level of the plateau both are influenced in a complex manner by the parameters R_G, C_{GS}, L_{SOURCE} and g_m. The expression in (4) for the linearized gate circuit of Fig. 5 gives an approximation for the time constant of the v_{GS} waveform between the level V_T and the level just prior to entering the ohmic region. With reference to Fig. 8, which will be described more fully later, during this very short turning-on interval, the mmf of the magnetic core does not change, and this effect may be represented by the constant-current generator I_{LM}. Thus, the boundary level for v_{GS} between the active and ohmic regions may be determined by using (1b), letting i_D' take on the peak value of diode current at the end of the diode reverse recovery interval, and solving for v_{GS}. Using the subscript A to correspond to this condition and rearranging (1b),

$$V_{DS,A} = \sqrt{\frac{I_{D,A}}{nk}} + V_T \tag{6}$$

Since the time constant τ_{A2} is relatively long compared to the plateau duration, the slope may be considered constant to a first-order approximation, and this time duration may be obtained from the relationship:

$$t_{PLATEAU} = \tau_{A2}\left[\frac{V_{GS,A} - V_T}{V_{DRIVE,ON} - V_T}\right] \tag{7}$$

By adding to the elementary gate-circuit model of Fig. 5 equivalent circuit models for the transformer and the input and output circuits, equations may be developed to obtain rough estimates of the plateau level of v_{DS} during turning-on. Figure 8 contains the essential elements for such an analysis. Since during the very short transition for the MOSFETs from ON to OFF and OFF to ON states the mmf of the core essentially is conserved, the magnetizing inductance may be replaced with a constant-current generator indicated by source I_{LM}. This equivalent replacement for the magnetizing inductance L_M has the value of the reflected secondary current at the begin-

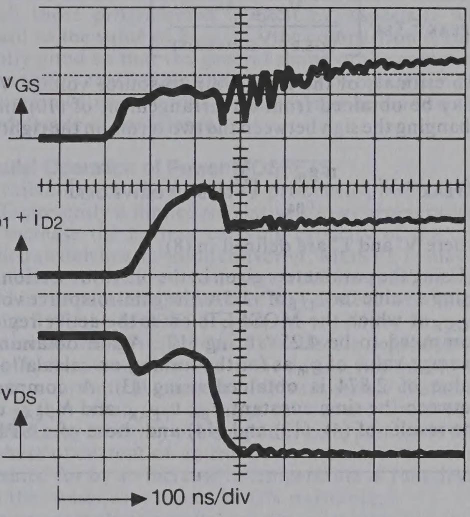

Figure 7. Oscillogram of turning-on interval. Vertical scale factors same as Fig. 2.

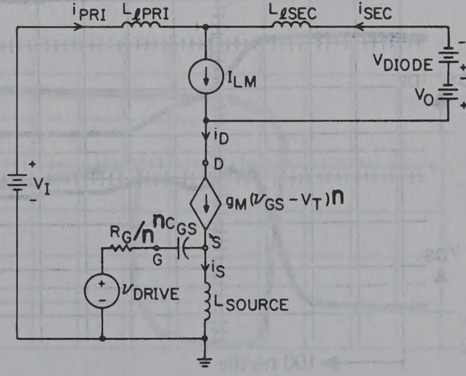

Figure 8. Simplified circuit model for piecewise linear analysis of drain-to-source voltage during turning-on and turning-off intervals.

$$V_{GS} = \begin{cases} V_{DRIVE,OFF} + [V_{DRIVE,ON} - V_{DRIVE,OFF}]e^{-t/\tau_{02}} & \\ \text{where } v_{GS} - V_T > V_{GS,B} - V_T & (11a) \\ V_{DRIVE,OFF} + [V_{GS,B} - V_{DRIVE,OFF}]e^{-t/\tau_{A4}} & \\ \text{where } 0 < v_{GS} - V_T < V_{GS,B} - V_T & (11b) \end{cases}$$

$$\text{and } V_{GS,B} = \sqrt{\frac{I_{D,B}}{nk}} + V_T \qquad (12)$$

An approximate expression for the time duration of the peak voltage V_{PEAK} between drain and source may be obtained by considering the slope to be constant and choosing a time constant based on an average value of transconductance between the maximum value corresponding to $V_{GS,B}$ and zero as the MOSFETs reenter the OFF region. The expression for this time is given by:

$$t_{PEAK} = \tau_{B4}\left[\frac{V_{GS,B} - V_T}{V_{GS,B} - V_{DRIVE,OFF}}\right] \qquad (13)$$

An estimate of the peak drain-to-source voltage V_{PEAK} may be obtained from a rearrangement of (10) and by changing the sign between the two terms on the right side.

$$V_{PEAK} = V' + \frac{n\, g_m L'}{\tau_{B4}}[V_{GS,B} - V_{DRIVE,OFF}] \qquad (14)$$

where V′ and L′ are defined in (8).

Using the parameters given in the previous section, and using a value for $I_{D,B}$ of 11.5A, the gate-to-source voltage $v_{GS,B}$ at which the MOSFETs enter the active region is computed to be 4.25V using (12). Again obtaining an average value of g_m as for the turning-on calculations, a value of 2.874 is obtained using (3). A comparison between the time constant τ_{B4}, t_{PEAK}, and V_{PEAK} using the results of (4), (13) and (14) and those of a SPICE2 simulation is shown below:

	LINEAR ANALYSIS	SPICE2
τ_{B4}	1226 ns	1800 ns
t_{PEAK}	557 ns	700 ns
V_{PEAK}	330 V	325 V

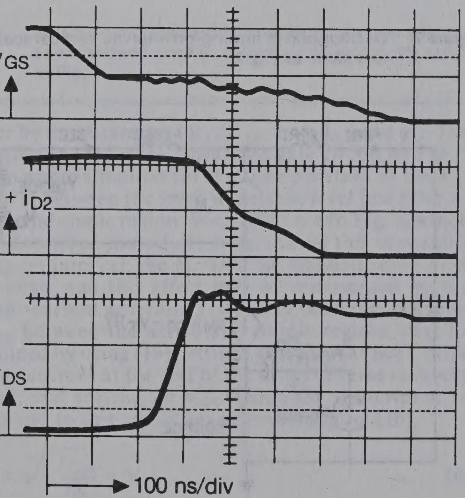

Figure 10. Oscillogram of turning-off interval. Vertical scale factors same as Fig. 2.

A comparison of the waveforms of total drain current and drain-to-source voltage as the source-lead inductance is varied is made in Figs. 11 and 12. In Fig. 11, the simulation results illustrate the differences which are particularly noticeable between the two waveforms of v_{DS}. With a 200 nH source-lead inductance in the simulation run of Fig. 11(a), the plateau level is higher and of longer duration in the turning-on interval than that in Fig. 11(b) or L_{SOURCE} of 100 nH. The higher plateau level due to the larger inductance causes an increase in power dissipated in the MOSFET during the turning-on interval. In general, it is not certain that more power always will be

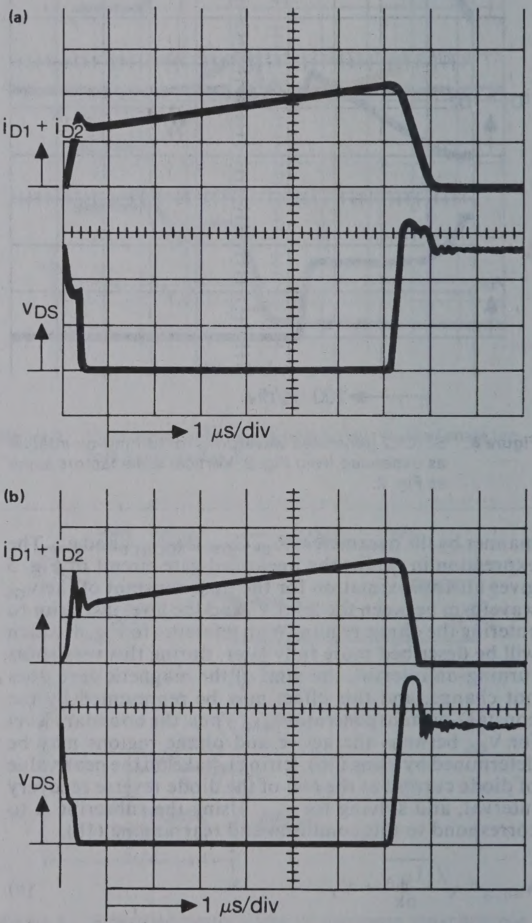

Figure 11. SPICE2 generated switching waveforms with (a) L_{SOURCE} = 200 nH and (b) L_{SOURCE} = 100 nH. Vertical scale factors: $i_{D1} + i_{D2}$, 5A/div; v_{DS}, 100V/div.

dissipated in the turning-off interval with the larger source-lead inductance, even though the turning-off time t_{PEAK} is longer than that for the lower 100 nH inductance. The reason for the uncertainty is that while the lower inductance reduces the turning-off time, the drain-source voltage is higher while current is still flowing in the drain circuit.

The effect of the source-lead inductance produces opposite effects at the two ends of the conduction period. While reducing the losses during the turning-on interval by lowering the source lead inductance, the peak drain-to-source voltage increases during the turning-off interval. Thus, attention to topological layout of the converter may result in reducing losses at the beginning of the conduction cycle, while adding unwanted voltage stress at the end of this period. Examination of the oscillograms of the experimental circuit in Fig. 12(a) and 12(b) shows the same effects observed in the simulation study. In the experimental converter, a length of wire was used in a rectangular geometric form to provide a one-turn loop. Variation of the inductance was accomplished by lengthening the rectangular loop. Measurements of the values of inductance were made using a controlled rate of rise of current through the loop while observing the L di/dt voltage across the loop. The source inductance corresponding to Fig. 12(a) was 192 nH, while that of Fig. 12(b) was 128 nH.

Summarizing this section, the same linear equivalent circuit used to analyze the turning-on interval is used as a model for obtaining expressions for estimates of time constants, peak drain-to-source voltage, and time duration of the peak voltage. In both the turning-on and turning-off analyses, an averaged value of transconductance g_m is used which is arbitrarily taken to be one-half of the transconductance at the boundary between the active region and the ohmic region. Since different amounts of current flow in the drain circuit at turning-on and turning-off times, the value of g_m used in the computations is different for the two intervals.

A study of the switching trajectory in Fig. 13, which was obtained by plotting i_D' versus v_{DS} from the SPICE2 simulation data of Fig. 2(b), reveals clearly the two regions of similar circuit behavior. The essentially vertical portions of the trajectory correspond to the turning-on plateau (approximately 160V) and the turning-off peak (approximately 325V). The i_D' versus v_{DS} trajectory of the experimental circuit is shown in Fig. 14. Although the conditions in the experimental circuit do not match in detail those programmed in SPICE2, especially with regard to the value of L_{SOURCE}, the comparison is sufficiently good so that the general shape of the computed trajectory is reasonable and estimates of maximum and minimum values of circuit variables may be made with a good degree of confidence.

Parallel Operation of Power MOSFETS

Availability of commercially produced power MOSFETs presently is limited to relatively low current ranges. To increase the current carrying capacity of the controlled switch in a dc-to-dc converter, MOSFETs may be connected in parallel with fewer problems than encountered in the parallel operation of BJT devices. In contrast to the BJT, the MOSFET possesses a positive temperature coefficient of resistance. This effect is dependent on the effective or rms current in the device, not the instantaneous current. The benefit of this resistance characteristic is that when two or more devices are operated in parallel, any tendency of a single device to pass more than its share of current on an rms current basis will be compensated for by an increase in temperature of that device and the consequent rise of its ON resistance.

As an example of parallel operation, the waveforms of the sum of drain currents from three paralleled IRF305 MOSFETs and the drain-to-source voltage for a two-

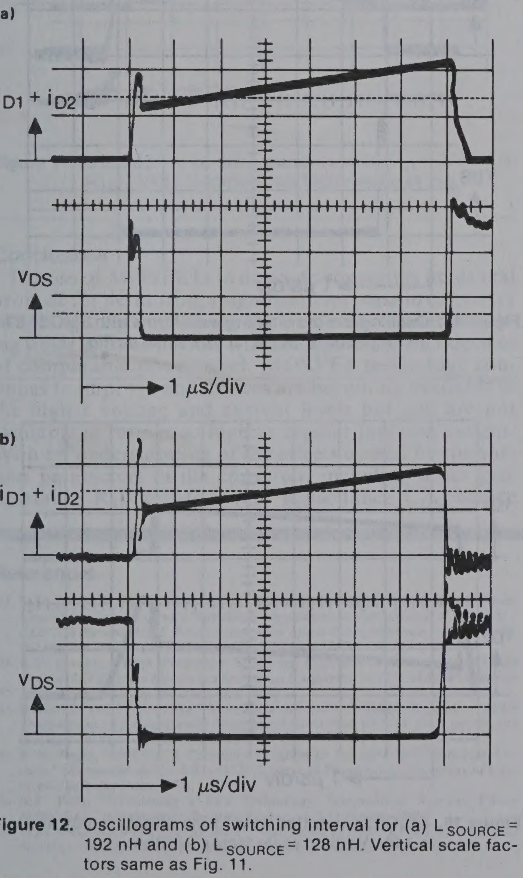

Figure 12. Oscillograms of switching interval for (a) L_{SOURCE} = 192 nH and (b) L_{SOURCE} = 128 nH. Vertical scale factors same as Fig. 11.

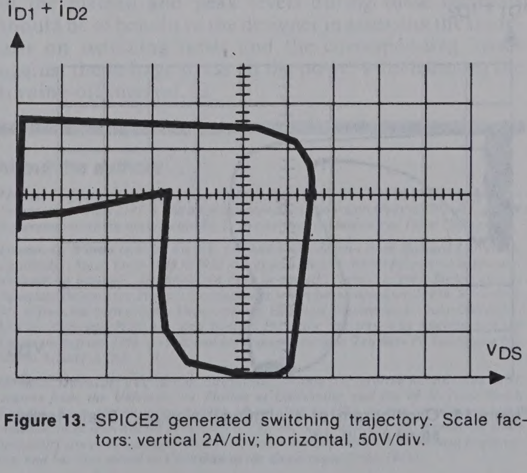

Figure 13. SPICE2 generated switching trajectory. Scale factors: vertical 2A/div; horizontal, 50V/div.

winding voltage-or-current step-up converter with an output power of 600W are shown in Fig. 15. The total peak current drawn by the three devices is approximately 12.5A and the maximum drain-to-source voltage at the turning-off time is approximately 375V. The absolute maximum ratings on a single device are 5A continuous drain current and 400V drain-to-source voltage. The MOSFETs for this experimental circuit were matched rather closely with respect to threshold voltage and transconductance.

Since the current-sharing effect depends upon temperature rise of individual devices due to the heating effect of the rms drain currents, current sharing on an instantaneous basis is not enforced. Current hogging during certain portions of a switching cycle may be caused by differences between devices in threshold voltage, gate circuit time constant, or transconductance. The time interval between applying the gate drive voltage and reaching the threshold level V_T is determined by the time constant τ_{02}, defined by (2), with the time delay being given approximately by the expression $\tau_{02}V_T/(V_{DRIVE,ON} - V_{DRIVE,OFF})$. Thus, variation in individual threshold voltages will prevent all of the MOSFETs in a parallel configuration from initiating conduction at the same instant. Indicating progressively higher threshold voltage levels by adding a numerical subscript, assume that in a three-MOSFET circuit, Q_1 has the lowest V_T. The delay in reaching V_{T1} will be due to the combined input circuits according to (2). After Q_1 goes into conduction, the rate-of-rise of the common gate-to-source voltage is limited by the time constant predicted by (4) where n now equals one since only one MOSFET is conducting. The time delay before Q_2 with threshold voltage V_{T2} begins to conduct is determined by the time constant τ_{A2} plus the initial time delay due to the effect of τ_{02}. The delay in starting conduction in Q_3 is further influenced by an additional new time constant τ_{A2} for n = 2 which is longer than the original time constant for the single MOSFET Q_1.

Waveforms of i_{D1} and i_{D2} from a SPICE2 simulation in which two MOSFETs are connected in parallel with V_{T1}= 3V and V_{T2}= 1V are shown in Fig. 16. The simulation run considers only the threshold effect and does not take into account any tendency toward rms current leveling due to temperature effects. However, even with the temperature-dependent resistance compensation inherent in the MOSFET characteristics, variation among device threshold voltages can cause this same effect in an actual circuit. The range of 1V to 3V was chosen to illustrate the maximum spread expected in V_T for the IRF305 device.

The effect of changes in time constant of the gate circuit due to parameters external to the MOSFET devices is also important. In Fig. 17, waveforms of drain current from the experimental circuit using two MOSFETs are shown where R_{G1}= 220Ω and R_{G2}= 100Ω. This combination allows Q_2 to conduct first due to the lower time constant τ_{02} for that MOSFET alone. After Q_2 commences conduction, the time constant affecting the entry into the active region by Q_1 is essentially that of τ_{A2} due to Q_2 already being in the active region.

Following the command from the gate-drive voltage to terminate the on-time, the time constant $\tau_{04} = \tau_{02}$ is in effect once more for the individual MOSFET Q_2 and it is turned off earlier than Q_1, which is then further delayed by time constant τ_{B4} due to the Q_1 circuit only. Figure 18 is a display of a SPICE2 simulation in which R_{G1}= 200Ω. In both the experimental and the simulated waveforms, an interesting effect not predictable by the simplified linear analysis is seen following the initial turn-off of Q_2. Although Q_2, which has the lower gate circuit time con-

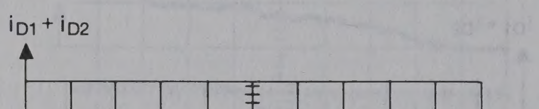

Figure 14. Oscillogram of switching trajectory. Scale factors same as Fig. 13.

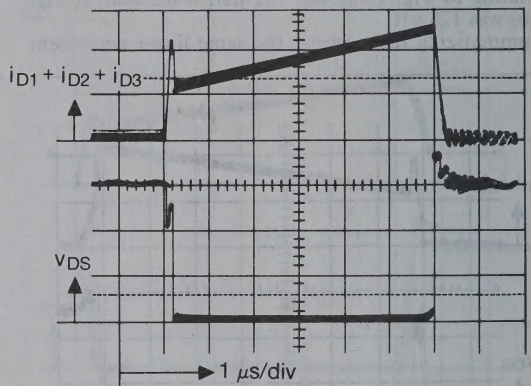

Figure 15. Oscillogram of switching waveforms with 3 MOSFETs and P_0= 600W. Scale factors same as Fig. 11.

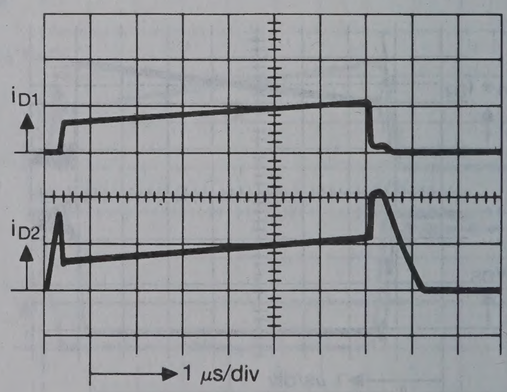

Figure 16. SPICE2 generated waveforms with V_{T1}= 3.0V and V_{T2} = 1.0V. Vertical scale factor: 2A/div.

stant, has been turned off initially, as the current through Q_1 begins to fall in the active region, the feedback voltage across the source-lead inductance is sufficiently high to charge the gate-to-source capacitance C_{GS2} of Q_2 back above V_T and to turn Q_2 on again briefly.

In an ideal situation without distributed inductive and capacitive effects and with a zero-impedance voltage-drive circuit, there would exist none of the problems of instantaneous current sharing just discussed. Even if the source impedance of the drive circuit were made zero, there is still a potential problem in the parallel connection of two or more devices capable of power amplification. Due to distributed inductive and capacitive effects, it is quite possible to have the circuit behave as an oscillator due to the parasitic elements. Resonant circuits formed by connection leads, particularly those in the drain and gate circuits, can lead to self-oscillations at very high frequencies as the power switch is driven into the active region. The insertion of loss elements into these distributed resonant circuits usually will solve the parasitic-oscillation problem. A commonly accepted technique is the one employed in this paper in which series resistive elements R_{G1}, R_{G2}, are placed in the gate circuit. Another method which is also used with success depends on the placement of ferrite beads on leads to add both inductive and resistive effects at the insertion points of the circuit. The addition of extra inductance aids in separating the self-resonant frequencies in the drain and gate circuits, thus reducing the possibility of regenerative feedback and parasitic oscillation.

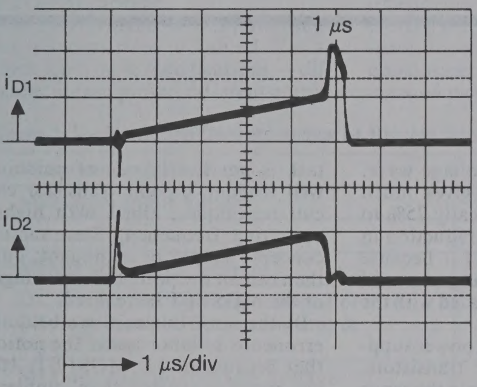

Figure 17. Oscillogram of drain currents with $R_{G1} = 220\Omega$ and $R_{G2} = 100\Omega$. Vertical scale factor same as Fig. 16.

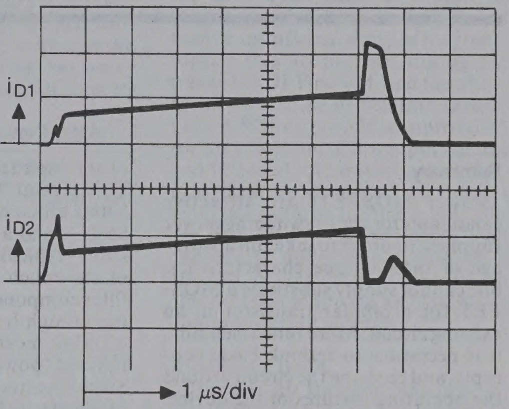

Figure 18. SPICE2 generated waveforms with $R_{G1} = 200\Omega$ and $R_{G2} = 100\Omega$. Vertical scale factor same as Fig. 16.

Conclusions

The use of MOSFETs in dc-to-dc converters holds real promise for permitting a significant increase in converter switching frequency due to the inherently shorter switching times of these devices when compared to BJT devices of comparable power level. MOSFET technology continues to improve and devices are becoming available in the higher voltage and current levels but still are not available in ratings as high as bipolar junction devices. With an understanding of the effects caused by the various parameters in the converter, including series gate resistance R_G, gate-to-source capacitance C_{GS}, source lead inductance L_{SOURCE}, and transconductance g_m, it is possible to design a system using paralleled MOSFET devices to increase the power handling capability of a dc-to-dc converter. The analytical relationships developed in the paper between the various time constants which partially describe a converter during the turning-on and turning-off intervals, and which provide estimates of the plateau and peak levels during these intervals should be of benefit to the designer in assessing the trade-offs on switching times and the corresponding losses against the voltage stress on the power switch during the turning-off interval. ☐

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Harry A. Owen, Jr. *was born in Hawthorne, Florida. He received his BEE and MSE degrees from the University of Florida at Gainesville, and his Ph.D. from North Carolina State University at Raleigh. From 1948 to 1951, he was an instructor and Assistant in Research at the University of Florida. Mr. Owen, a faculty member of Duke University since 1951, is currently a Professor in the Department of Electrical Engineering, and has also served as Chairman of the Department (1968-1974).*

CHAPTER 7
APPLICATION NOTE 939

A Universal 100kHz Power Supply Using a Single HEXFET™

By **S. CLEMENTE, B. PELLY, R. RUTTONSHA,** International Rectifier Applications Engineering Department

Summary

Power MOSFETs are attractive candidates for use in switching power supplies. In order to take full advantage of their unique characteristics, one cannot simply substitute a MOSFET for a bipolar transistor in an existing circuit. More fundamentally, it is necessary to rethink basic concepts, and to shape the circuit around the operating features of the device.

This application note describes a 100kHz, 100W off-line power supply providing a regulated 5V DC output. The circuit is "universal" in the sense that it operates both from 115V and 240V line inputs, without any alteration of circuitry or switching of components. The circuit uses a single 500V-rated power HEXFET in a modification of the classical "forward converter" circuit.

Introduction

DC power supplies are employed today wherever electrical or electronic equipment is in use. Traditional designs that operate from AC input power are based upon the use of a line frequency transformer, a secondary rectifier, an output filter and a dissipative series regulating element; typical overall efficiency is 40% to 50%.

Newer designs are based upon fundamentally more efficient high frequency switching techniques. The line frequency is first rectified to DC, then inverted to high frequency AC, by a transistor switching circuit. The high frequency voltage is fed through an output transformer, rectified and filtered to produce the required DC. Regulation of the output is accomplished by controlling the pulse width of the high frequency voltage wave. This circuit technique gives much better efficiency — typically 75% to 85% — and a dramatic reduction in size — typically 4 or 5 to 1 — because of the much smaller magnetic and filter components associated with the use of high frequency.

Today, most switching power supplies use power bipolar transistors. Switching frequencies are in the range of 20kHz to 40kHz. Although a few designs operate at higher frequency, this undoubtedly means "pushing" the bipolar to the limits of its performance.

Higher operating frequency than the usual 20kHz to 40kHz range is in principle advantageous, because it offers the possibility for further reductions in size of magnetic and filter components, as well as faster response. With the availability of power MOSFETs, the switching component is no longer the frequency limiting element in the system. This new situation has generated considerable interest in where the optimum switching frequency of a power supply now lies, having due regard to the technology of the associated magnetic and filter components. Presently, there is no clear consensus. It is safe to say, however, that the optimum switching frequency is certainly greater than the 20kHz to 40kHz range of the bipolar transistor. Most probably it is at least 100kHz, and perhaps considerably higher.

It would be erroneous, however, to assume that the potential advantage of the power MOSFET is simply one of faster switching speed and higher frequency. In order to utilize all of the characteristics of the power MOSFET to best advantage, the design task is not simply one of pursuing well trodden bipolar transistor circuit techniques, albeit with higher operating frequency. Basic circuit concepts should be rethought; only then can all the potential advantages of the MOSFET be realized.

By the same token, it can be quite erroneous to labor under the notion that because power MOSFETs still are more expensive than bipolars, therefore they are not yet economically competitive. This overlooks the fact that performance advantages, or cost reductions, or both, are achieveable at the system level with these devices, that can more than compensate for their higher costs.

In this application note, we present a switching power supply using a HEXFET that operates at 100kHz — a considerably higher frequency than normally used with bipolar transistors. Attainment of this frequency actually is no particular feat for a power HEXFET, since frequencies much higher are within easy reach. A more vital objective of this application note is to demonstrate that by rethinking basic circuit concepts, results are achievable which, to many circuit designers at first sight, might seem to be unattainable. Specifically, we will show that just a single 500V-rated HEXFET can be used in a circuit that operates from a 265V line input; this compares with the usual 800V minimum rating requirement of a bipolar transistor in a single-ended circuit. We will moreover demonstrate a circuit which has the surprising capability of maintaining a constant DC output voltage over a very wide range of line input voltage — a "universal" power supply — that can operate both from the 115V line common in the United States, and from a 220V/240V line common in Europe, without any modification of circuitry or switching of components.

Specific Design Goals

The discussion that follows is addressed to the general circuit concepts involved in using a single power HEXFET in a wide input voltage range switching power supply. A specific implementation of the concepts described is presented; this is a circuit for a 100kHz, 100W, 5V DC power supply that employs a single 500V/3.5A-rated power HEXFET in a TO-220 package.

The performance of this power supply is summarized in Table 1. Variations from these specifications — different output power, different output voltage, different operating frequency, and so on — are obviously possible, without departing from the basic concepts.

Basic Concepts

The Conventional Forward Converter Circuit

The basic single-transistor forward converter circuit is shown in Figure 1. Idealized voltage and current waveforms that describe the operation are shown in Figure 2. During the conduction period of the transistor, current is transferred from the primary DC power source through the output transformer to the output circuit. During the OFF period of the transistor, the magnetizing current in the transformer is returned via the clamping winding to the primary DC source, resetting the flux in the transformer core, prior to the next cycle of operation.

Table 1. Performance Characteristics of 100kHz "Universal" Power Supply

Minimum Input Voltage	85V RMS, 50-400 Hz
Maximum Input Voltage	265V RMS, 50-400 Hz
Output Voltage	5V DC
Maximum Output Current	20A DC
DC Output Voltage Regulation, For All Conditions of Output Current & Input Voltage	± 0.5%
Maximum Output Ripple Voltage	50mV P-P
Transient Response for a Step Change of 10A Load Current	500mV, settling within 250μs
Full Load Efficiency	74%

The clamping winding usually has the same number of turns as the primary, which means that the peak voltage developed across the transistor during the OFF period is twice the primary DC supply voltage. For a nominal line input voltage of say 240V, this peak voltage would be about 720V; this is why a transistor voltage rating of at least 800V is required.

The maximum permissible conduction period of the transistor is 50% of the total cycle time. It cannot be longer than this, because there would then be insufficient time for the transformer flux to be reset during the transistor OFF period, and the transformer would be driven into saturation. A 50% duty cycle is approached for the condition of low input voltage and full load; the transistor conduction time automatically decreases from this point as the line input voltage increases or as the output load decreases, under the action of a closed-loop regulator circuit, which acts so as to maintain an essentially constant output voltage.

Modified Circuit

There is no fundamental need to clamp the peak transistor voltage to twice the supply voltage. The device voltage could be clamped to any level that is higher than the DC supply

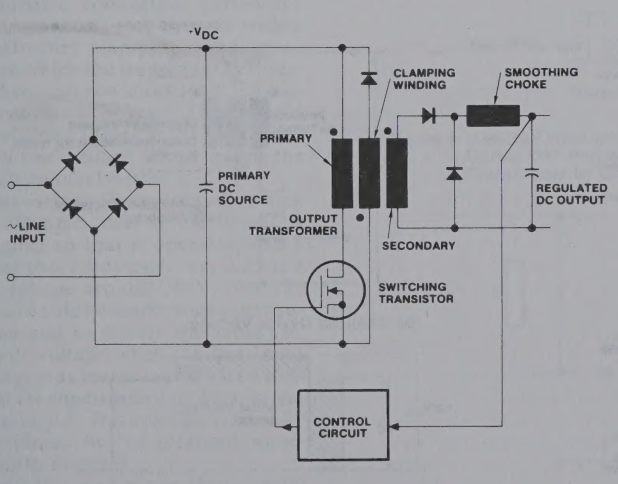


Figure 1. Basic Single-Transistor Forward Converter Circuit

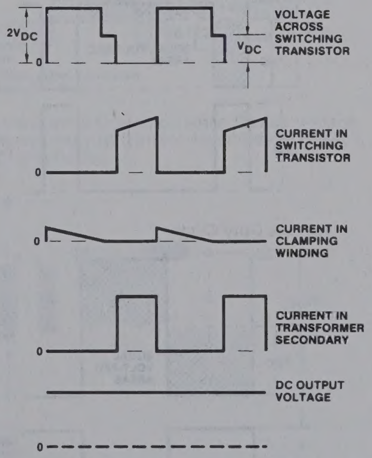


Figure 2. Idealized Waveforms for the Circuit of Figure 1

voltage, so long as the voltage-time integral developed across the transformer during the OFF period of the transistor is equal and opposite to the voltage-time integral during the conduction period, thereby fully resetting the flux by the end of each cycle.

It is therefore possible, in principle, to reduce the peak transistor voltage, at the expense of reducing the conduction time of the transistor. The penalty is that the peak device current necessarily increases as the conduction time decreases, for a given power output and input voltage level. The idealized waveforms in Figure 3(a) illustrate operation with a 20% duty cycle; for comparison, Figure 3(b) represents operation with a 50% duty cycle, for the same power output and input voltage. The peak transistor current is greater by a factor of 2.5 for the shorter conduction period; the peak transistor voltage, on the other hand, is lower, by a factor of 1.6. This means that for a 240V input, the peak transistor voltage is reduced from the usual 720V to around 450V, permitting a 500V-rated HEXFET to be used.

With a bipolar transistor, operation with a duty cycle substantially less than 50% is undesirable. The gain of a bipolar decreases, and the device becomes increasingly difficult to use as the peak current increases. The transconductance of the power HEXFET, on the other hand, does not decrease with increasing drain current, and it is quite practical to operate a HEXFET with a short duty cycle at relatively high peak current. Higher peak current will, of course, produce greater conduction power dissipation than would be obtained in a circuit operating with a longer conduction time at correspondingly lower current. This is of little concern, however, because the HEXFET is well able to handle the "extra" dissipation; in any event, the dissipation in the switching device is substantially less than that in the output rectifiers. It is an unfortunate fact that the conduction voltage drop in these rectifiers is quite significant for a 5V output, and the circuit losses tend to be dominated by the rectifier losses.

Clamping the Drain Voltage

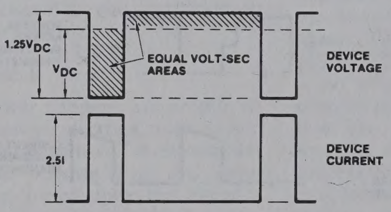
The drain voltage must be clamped at a level that ensures the output transformer is completely reset during the OFF period of the HEXFET. There are various ways of doing this.

A clamping winding on the output transformer — used in the conventional forward converter with a 50% duty cycle — can, in principle, still be used. The ratio of clamping turns to primary turns would, of course, no longer be 1 to 1. Taking the example considered, for a conduction duty cycle of 0.2, the peak transistor voltage must be at least 1.25X the primary DC source voltage. The clamping winding should therefore have four times the number of primary turns, as shown in Figure 4(a).

This fixes the peak transistor voltage at 1.25X the primary DC source voltage, as illustrated in Figure 4(b). A duty cycle of 0.2 would be set to occur when the line input voltage is lowest, and the output load current is highest. As the line input voltage increases, or the load current decreases, the conduction time of the transistor would decrease, under the action of a closed-loop regulator, so as to keep the DC output voltage at a constant value. The transistor clamping voltage would always be 1.25X the primary DC source voltage, regardless of what that voltage might be. The flux in the transformer is therefore reset before the end of the cycle, except at the condition of minimum line input voltage, and the peak transistor voltage is therefore generally higher than the level that is just sufficient to reset the transformer by the end of the cycle.

A transformer clamping winding, though realizable, creates some practical problems. In the example considered, the peak voltage developed between the primary and clamping windings would be five times the DC source voltage; the insulation between these windings must be sufficient to withstand this voltage. The clamping rectifier also sees a total of five times the DC source voltage and must be rated accordingly. Perhaps the biggest practical difficulty is that

(a) 20% Duty Cycle



(b) 50% Duty Cycle

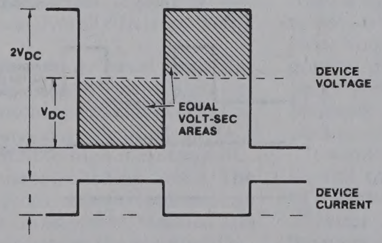
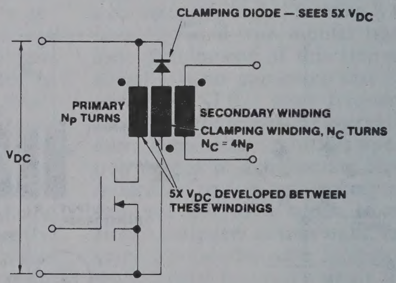


Figure 3. Idealized Waveforms of Device Voltage and Current

(a) Circuit


CLAMPING DIODE — SEES 5X V$_{DC}$
PRIMARY N$_P$ TURNS
SECONDARY WINDING
CLAMPING WINDING, N$_C$ TURNS
N$_C$ = 4N$_P$
V$_{DC}$
5X V$_{DC}$ DEVELOPED BETWEEN THESE WINDINGS

(b) Idealized Device Voltage

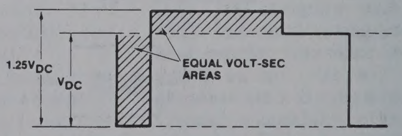


Figure 4. Use of a Transformer Clamping Winding

substantial leakage inductance and self-capacitance inevitably appears between the primary and clamping windings, and this gives rise to superimposed high frequency oscillations on the current and voltage waves, as shown in Figure 4(c). These oscillations are difficult to eliminate.

A Different Approach

A much more satisfactory approach arises from the basic fact that for minimum voltage stress on the HEXFET, the voltage that appears across the transformer during the device OFF period should have the right amplitude to reset the flux just by the end of this period, independent of the conduction duty cycle. This principle is illustrated by the idealized waveforms in Figure 5. In this example, it is assumed that the minimum duty cycle, which occurs at maximum input voltage, is 0.15.

If this principle is followed, the voltage that appears across the transformer during the reset period by no means bears a fixed relationship to the primary DC source voltage; it increases as the DC source voltage decreases and is inversely proportional to (1-D), where D is the duty cycle. Thus, a transformer clamping winding, in principle, will not do the job.

If the required clamping circuit could be devised, two benefits — in addition to the elimination of the transformer clamping winding — would be realized. First, as already mentioned, the voltage across the HEXFET would be minimized. Second, there would not be a maximum permissible conduction period for the transistor — as there is with a transformer clamping winding — above which the transistor OFF period becomes too short for the transformer flux to be reset. There would therefore no longer be the same minimum line voltage below which the circuit cannot operate.

This is very interesting; it means, for example, that if the circuit is designed so that it operates with a rather short duty cycle, say 0.15 at a line voltage around 265V, then the circuit could be made to stay in regulation and to deliver the same DC output voltage when the line input voltage is as low as say 80V, at which point the conduction duty cycle would be about 0.5. This example is actually represented by the idealized waveforms in Figure 5.

Even this would not theoretically be the limiting range of operation; as a practical matter, however, most integrated circuits that are intended for controlling power supplies of this type have a maximum duty cycle of 0.5. At all events, if we design the circuit according to these principles, we will have a "universal" power supply, capable of delivering the same regulated DC output voltage both from 115V and 220V/240V line inputs, with no modification of circuitry, or switching of components.

A Capacitor-Resistor-Diode Clamp

The desired clamping circuit can be realized in a surprisingly simple manner. The circuit is illustrated in Figure 6. The capacitor C is a "reservoir" capacitor which charges to an essentially steady level of voltage — the necessary transformer resetting voltage. The resistor R dissipates the energy delivered to the clamping circuit from the transformer. Unlike the transformer winding, which returns the energy stored in the transformer to the primary DC source, this is a dissipative clamp.

(c) Practical Oscillograms

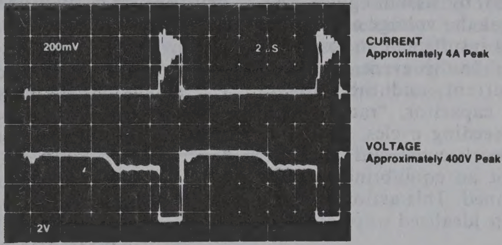


Figure 4. Use of a Transformer Clamping Winding (continued)

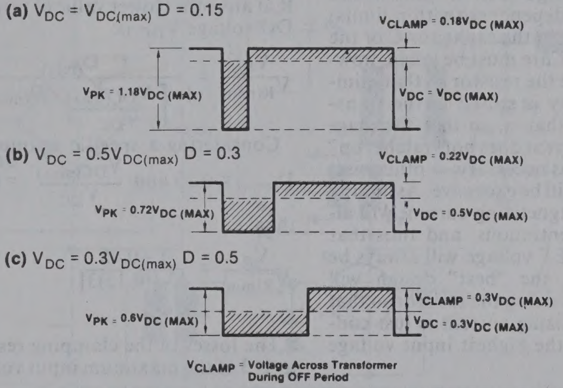

(a) $V_{DC} = V_{DC(max)}$ D = 0.15
$V_{CLAMP} = 0.18V_{DC\,(MAX)}$
$V_{PK} = 1.18V_{DC\,(MAX)}$
$V_{DC} = V_{DC\,(MAX)}$
(b) $V_{DC} = 0.5V_{DC(max)}$ D = 0.3
$V_{CLAMP} = 0.22V_{DC\,(MAX)}$
$V_{PK} = 0.72V_{DC\,(MAX)}$
$V_{DC} = 0.5V_{DC\,(MAX)}$
(c) $V_{DC} = 0.3V_{DC(max)}$ D = 0.5
$V_{CLAMP} = 0.3V_{DC\,(MAX)}$
$V_{PK} = 0.6V_{DC\,(MAX)}$
$V_{DC} = 0.3V_{DC\,(MAX)}$
V_{CLAMP} = Voltage Across Transformer During OFF Period

Figure 5. Idealized Waveforms Illustrating Operation when Device Voltage During OFF Period Always has just Correct Amplitude to Reset Transformer by End of this Period.

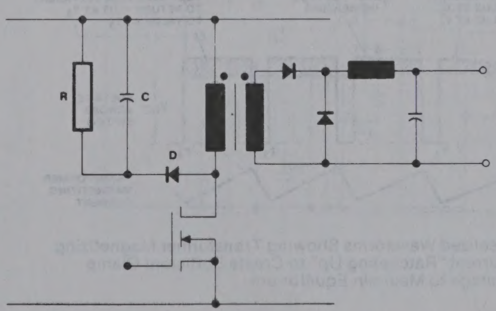


Figure 6. Capacitor-Resistor-Diode Clamp

From a practical point of view, because of the possibility for operating at high frequency, the transformer can be designed so that the power dissipation in the clamp is kept to a quite acceptable level. In the specific circuit described, the power dissipation in the clamping circuit is quite minimal, and ranges between 2% and 3% of the output power.

The inherent action of this simple clamp can be arranged to be such as to adjust the steady-state voltage across the capacitor to the level required to reset the transformer just by the end of the OFF period, regardless of the level of input voltage. This can be seen by assuming for the moment that the voltage across the capacitor is insufficient to reset the transformer. In this event, the magnetizing current, and the voltage across the capacitor, "ratchet up" during succeeding cycles, until the voltage does become sufficient, at which point an equilibrium condition is attained. This action is illustrated by the idealized waveforms in Figure 7.

This clamp thus provides the required voltage to keep the transformer voltage-time integral within balance, independent (within limits) of the value of the capacitor C or the resistor R. Care must be taken, however, to size the resistor so that minimum energy is stored in the transformer — that is, so that the magnetizing current does not "ratchet up" more than is necessary — otherwise, the losses will be excessive. Assuming that the magnetizing current will always be continuous, and thus that the HEXFET voltage will always be minimized, the "best" design will result from sizing the resistor so that the magnetizing current is just continuous at the highest input voltage level.

The general relationship between the voltage across the clamping resistor, V_R, and the primary DC source voltage, V_{DC}, for a given conduction duty cycle, D, with continuous transformer magnetizing current is:

$$V_R = \frac{D\,V_{DC}}{(1\text{-}D)}$$

The required value of the resistor R is therefore given by:

$$R = \frac{\left[\dfrac{D_{(min)}\,V_{DC(max)}}{1\text{-}D_{(min)}}\right]^2}{\left[\tfrac{1}{2}\,L_{(mag)}\,I^2_{(mag)PK} + \tfrac{1}{2}\,L_S\,I^2_{LPK}\right]\,f}$$

Where $D_{(min)}$ is the minimum full load duty cycle, (obtained when $V_{DC} = V_{DC(max)}$).

$L_{(mag)}$ is the transformer magnetizing inductance.

$I_{(mag)PK}$ is the peak magnetizing current for just-continuous magnetizing current.

L_S is the leakage inductance of the transformer, referred to the primary.

I_{LPK} is the peak full load current in the transformer primary.

f is the frequency.

The ratio of the voltage V_R across R at any other lower value of primary DC voltage V_{DC} is:

$$\frac{V_R}{V_{R(min)}} = \frac{1 - D_{(min)}}{1 - \left[\dfrac{V_{DC(max)}}{V_{DC}} \cdot D_{(min)}\right]}$$

Considering a specific example, if

$$D_{(min)} = 0.15 \text{ and } \frac{V_{DC(max)}}{V_{DC}} = 0.3,$$

then:

$$\frac{V_R}{V_{R(min)}} = \frac{1 - 0.15}{1 - [(0.15)3]} = 1.55$$

The losses in the clamping resistor at 1/3 of the maximum input voltage would then be $1.55^2 = 2.4$X the losses at maximum input voltage.

The maximum power dissipation in the clamp — obtained at the lowest input voltage — can be reduced, at the expense of a small increase in the maximum voltage developed across the HEXFET — obtained at the highest input voltage — by sizing the resistor R so that the magnetizing current becomes discontinuous at some intermediate value of line input voltage. As the input voltage increases above this level, the peak magnetizing current stays constant, while the magnetizing current waveform becomes progressively more discontinuous, and the voltage across the clamp circuit stays constant, because (for a given load current) the energy stored in the transformer is constant. Below the critical intermediate level of line voltage, the transformer magnetizing current becomes continuous, and the clamping voltage rises as the input voltage decreases.

As an example of this design approach, assume that the clamp resistor is sized to give just-continuous conduction at 45% of maximum line voltage. If the minimum duty cycle at maximum input voltage is 0.15, then at maximum input voltage, the peak voltage developed across the transistor will be 1.23, instead of 1.18 times the primary DC source voltage. For a total range of input voltage variation of 3 to 1, the maximum duty cycle would be 0.45, and the ratio of the maximum to minimum voltage across the clamp resistor would be:

$$\frac{V_{R(max)}}{V_{R(min)}} = \frac{1 - (0.15/0.45)}{1 - 0.45} = 1.22$$

The range of maximum to minimum power loss in the clamp resistor at full output power would then be $1.22^2 = 1.49$. Figure 8 illustrates this specific design example.

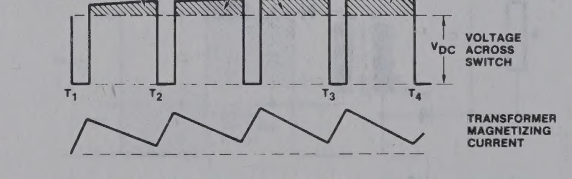

VOLT-SECS INSUFFICIENT TO RETURN FLUX AT T_2 TO VALUE AT T_1
CLAMP VOLTAGE INCREASING
VOLT-SECS NOW SUFFICIENT TO RETURN FLUX AT T_4 TO VALUE AT T_3
V_{DC}
VOLTAGE ACROSS SWITCH
T_1
T_2
T_3
T_4
TRANSFORMER MAGNETIZING CURRENT

Figure 7. Idealized Waveforms Showing Transformer Magnetizing Current "Ratcheting Up" to Create Sufficient Clamp Voltage to Maintain Equilibrium

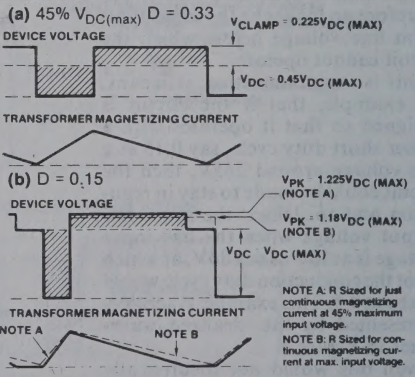

(a) 45% $V_{DC(max)}$ D = 0.33
DEVICE VOLTAGE
$V_{CLAMP} = 0.225V_{DC\ (MAX)}$
$V_{DC} = 0.45V_{DC\ (MAX)}$
TRANSFORMER MAGNETIZING CURRENT
(b) D = 0.15
DEVICE VOLTAGE
$V_{PK} = 1.225V_{DC\ (MAX)}$ (NOTE A)
$V_{PK} = 1.18V_{DC\ (MAX)}$ (NOTE B)
$V_{DC} = V_{DC\ (MAX)}$
TRANSFORMER MAGNETIZING CURRENT
NOTE A
NOTE B
NOTE A: R Sized for just continuous magnetizing current at 45% maximum input voltage.
NOTE B: R Sized for continuous magnetizing current at max. input voltage.

Figure 8. Idealized Waveforms Showing Operation when Clamp Resistor is Sized to Give just Continuous Magnetizing Current at 45% Maximum Input Voltage

Practical Circuit

Figure 9 shows a complete diagram for a 100W, 100kHz, 5V DC output circuit, which conforms with the performance specifications shown in Table 1. Component details are listed in Table 2.

Table 2. List of Components for Figure 9

Q1	IRF830 HEXFET
IC	Silicon General 3526
B1	IR 3KCB80
C1	500μF, 450V wkg.
C2	0.68μF, 100V
C3	4X 150μF, 6V
C4	22μF, 16V
C5	0.5μF, 25V wkg.
C6	10nF
C7	910pF
C8	0.0068 mfd.
C9	0.005μF
C10	0.1μF
C11	22μF, 25V
R1	1.5K (3X500Ω, 5W)
R2	12Ω 1/4W
R3	6.8kΩ 1/4W
R4	10Ω
R5	12kΩ 1/4W
R6	100Ω potentiometer
R7	33Ω 1/4W
R8	560Ω 1/4W
D1	20FQ030
D2	60HQ100
D3	IR 40SL6
Z1	1N4112 zener diode
Z2	1N4112 zener diode
Z3	4X 1N987B zener diodes in series
L1	Pan Magnetics International E-2481 (Core Arnold A-930157-2, 16 turns, 2 in parallel #14)
T1	Pan Magnetics International E-2478 (Core TDK 26/20. Primary: 20 turns, 3 in parallel #32; Secondary: 3 turns, 0.3mm x 0.8cm copper strip)
T2	Pan Magnetics International E-2479 (Core TDK H5B2T10-20-5. Primary: 6 turns #24; Secondary: 6 turns #24)
T3	Pan Magnetics International E-2480 (Core TDK H5B2T5-10-2.5. Primary: 1 turn; Secondary: 100 turns #32)

Performance Measurements

Oscillograms for various operating conditions are shown in Figures 10 through 20. Figure 10(a) and (b) shows oscillograms of drain voltage and drain current for output currents of 20A and 5A, respectively, with a 85V input. Figure 11(a) and (b) shows corresponding waveforms with 265V input.

Figure 12(a) and (b) shows oscillograms of HEXFET voltage and current during turn-ON for output currents of 20A and 5A, respectively, with 85V input. Note that although the voltage across the HEXFET falls in about 75ns, the rise time of the HEXFET current with a 20A output is over 300ns. This rather long rise time is due to leakage inductance, primarily of the transformer, and does not reflect the switching speed of the HEXFET. Figure 13(a) and (b) shows corresponding oscillograms for the turn-on interval, with 265V input. The rise time of the current is faster, because the higher voltage produces an increased rate-of-rise of current in the circuit inductance.

Figure 14(a) and (b) shows oscillograms of HEXFET voltage and current during turn-OFF for output currents of 20A and 5A, respectively, with 85V input. Transformer leakage inductance does not significantly effect the fall time of the current, because the current in the leakage inductance when switching OFF is diverted into the clamping circuit, and the slow fall time is not "seen" by the HEXFET. Figure 15(a) and (b) shows corresponding oscillograms during turn-OFF, with 265V input.

In Figures 11 and 15, it can be seen that with the maximum line input voltage of 265V, the peak voltage developed across the HEXFET at full load, including the voltage "spike" when switching OFF, is about 440V. This is comfortably within the 500V rating of the device.

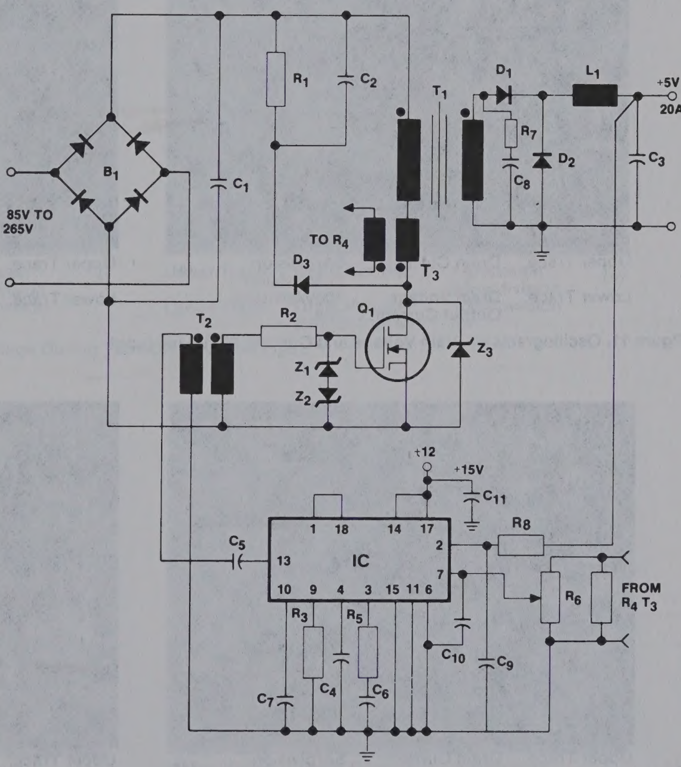
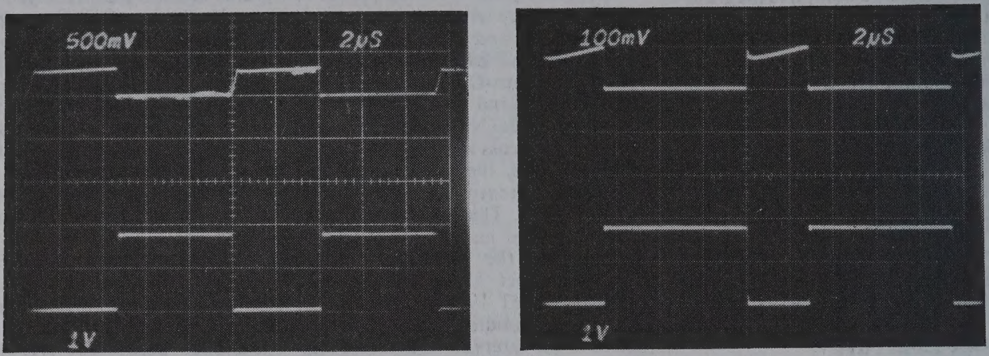


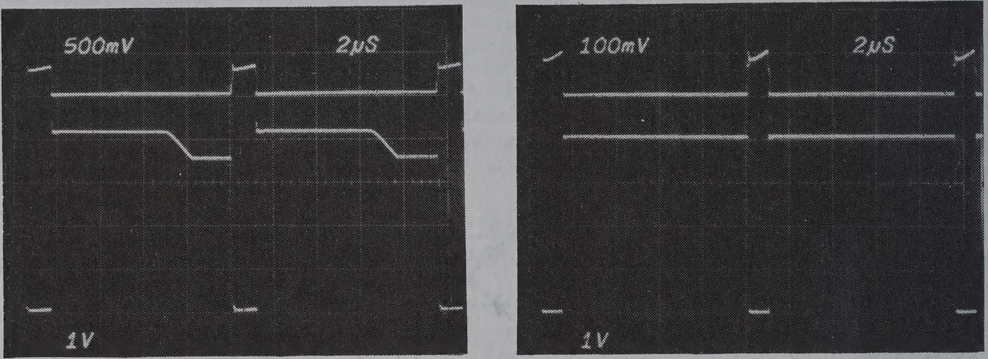
Figure 9. Circuit Diagram of 100kHz, 100W Wide Range Power Supply



Upper Trace: Drain Current: 5A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A
(a)

Upper Trace: Drain Current: 1A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A
(b)

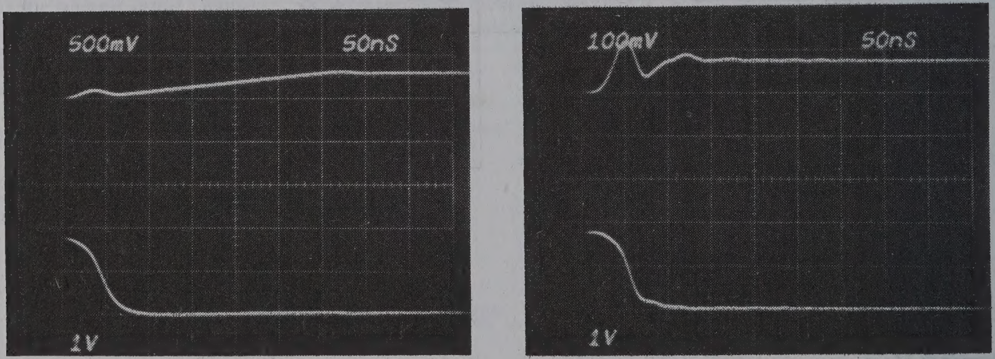
Figure 10. Oscillograms of Drain Voltage and Current, 85V Line Input



Upper Trace: Drain Current: 5A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A
(a)

Upper Trace: Drain Current: 1A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A
(b)

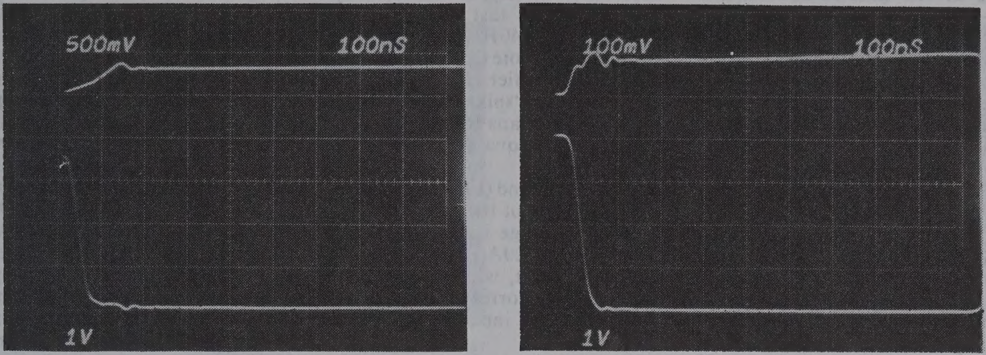
Figure 11. Oscillograms of Drain Voltage and Current, 265V Line Input



Upper Trace: Drain Current: 5A/division
50ns/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A
(a)

Upper Trace: Drain Current: 1A/division
50ns/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A
(b)

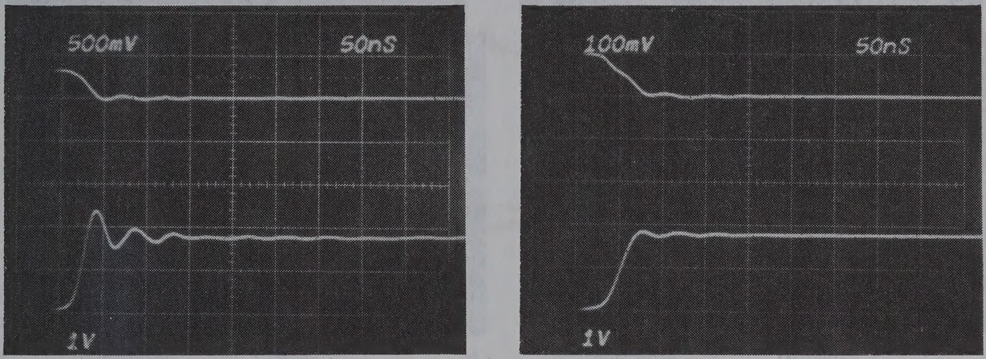
Figure 12. Oscillograms of Drain Voltage and Current During Turn-On, 85V Line Input



Upper Trace: Drain Current: 5A/division (a)
100ns/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A

Upper Trace: Drain Current: 1A/division (b)
100ns/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

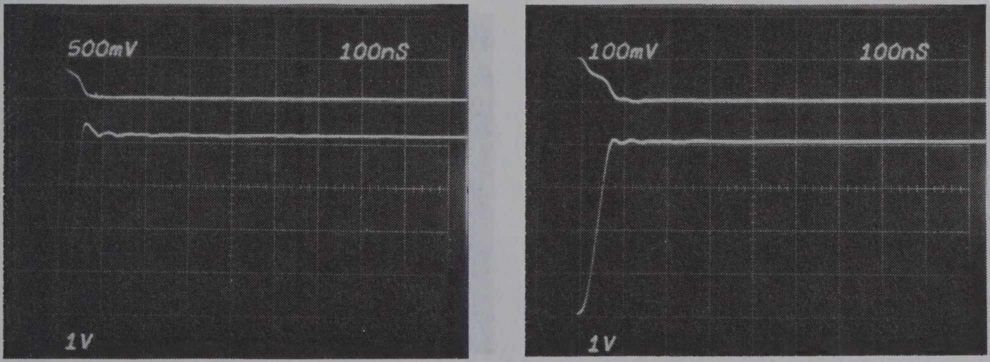
Figure 13. Oscillograms of Drain Voltage and Current During Turn-On, 265V Line Input



Upper Trace: Drain Current: 5A/division (a)
50ns/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A

Upper Trace: Drain Current: 1A/division (b)
50ns/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

Figure 14. Oscillograms of Drain Current and Voltage During Turn-Off, 85V Line Input



Upper Trace: Drain Current: 5A/division (a)
100ns/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A

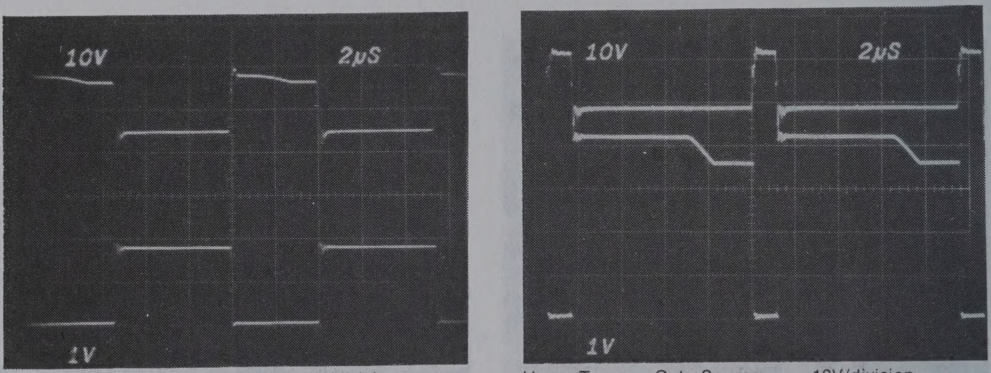
Upper Trace: Drain Current: 1A/division (b)
100ns/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

Figure 15. Oscillograms of Drain Current and Voltage During Turn-Off, 265V Line Input

Figure 16(a) and (b) shows oscillograms of the gate-to-source and drain-to-source voltages at line input voltages of 85V and 265V, respectively, with the full load output current of 20A, while Figure 17 shows oscillograms of voltage across the output rectifiers, D_1 and D_2, with 5A output current, for input voltages of 85V and 265V. Note that with 265V input, the voltage across the output freewheeling rectifier, D_2, including the transient commutation spike, is about 75V. An experimental 20A, 100V Schottky rectifier was used in this position. At the time of writing, this particular device is not yet commercially available; the 60A, 100V-rated 60HQ100 Schottky rectifier, though really oversized, is listed in Table 2, since it is commercially available. Alternatively, of course, an appropriate 100V fast recovery rectifier, such as the 40HFL100S02, could be employed. Note that the peak voltage across rectifier D_1, including the commutation "spike", is less than 20V, which means that a 30V-rated Schottky is adequate.

Figure 18(a) and (b) shows the transient response of the output voltage to a step change in output current from 10A to 20A, and vice versa, with 85V input, while Figure 19(a) and (b) shows corresponding oscillograms for 265V input.

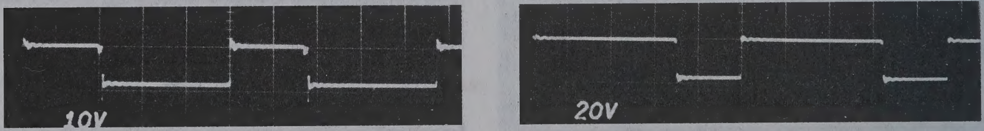
Figure 20(a) and (b) shows oscillograms of drain current and drain voltage with a short circuit applied at the output, at input voltages of 85V and 265V, respectively. With 85V input, the peak HEXFET current is regulated to about 3A, by the automatic current limiting facility built into the control circuit, and the corresponding DC output current is just over 20A. With 265V input, however, the peak HEXFET current is about 7A, the short circuit DC output current is about 55A, and the peak HEXFET voltage is almost 500V. The lack of effective current limiting under this condition is due to the fact that the control circuit has a minimum ON conduction time of about 0.8 microseconds, and this is not short enough to keep the current under control under short circuit conditions.



Upper Trace: Gate-Source Voltage: 10V/division 2μs/division (a)
Lower Trace: Drain Voltage: 100V/division
Line Input: 85V

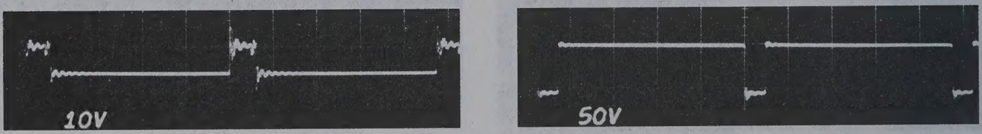
Upper Trace: Gate-Source Voltage: 10V/division 2μs/division (b)
Lower Trace: Drain Voltage: 100V/division
Line Input: 265V

Figure 16. Oscillograms of Gate-Source Voltage and Drain Voltage, 20A Output



Voltage across D1: 10V/division (a)
2μs/division
Input: 85V

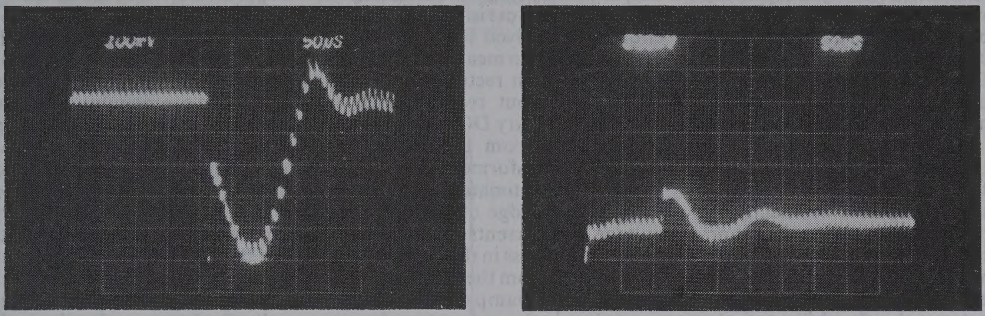
Voltage across D2: 20V/division (b)
2μs/division
Input: 85V



Voltage across D1: 10V/division (c)
2μs/division
Input: 265V

Voltage across D2: 50V/division (d)
2μs/division
Input: 265V

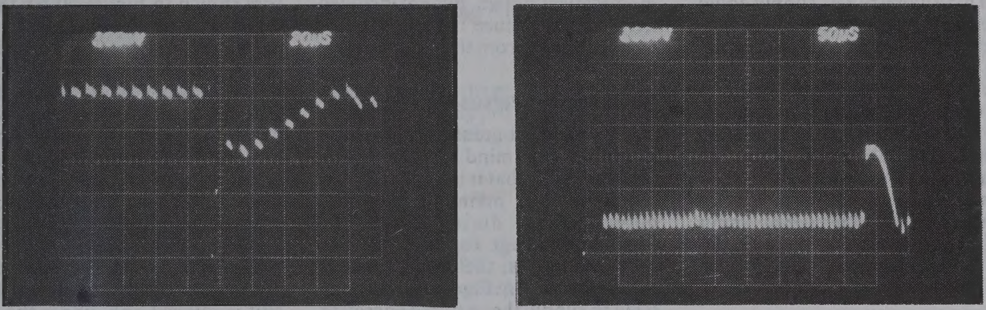
Figure 17. Oscillograms of Voltage Across Output Rectifiers D1 and D2, 5A Output Current



Output Voltage: 100mV/division
50μs/division
Step Load
Change: 10A to 20A
(a)

Output Voltage: 100mV/division
50μs/division
Step Load
Change: 20A to 10A
(b)

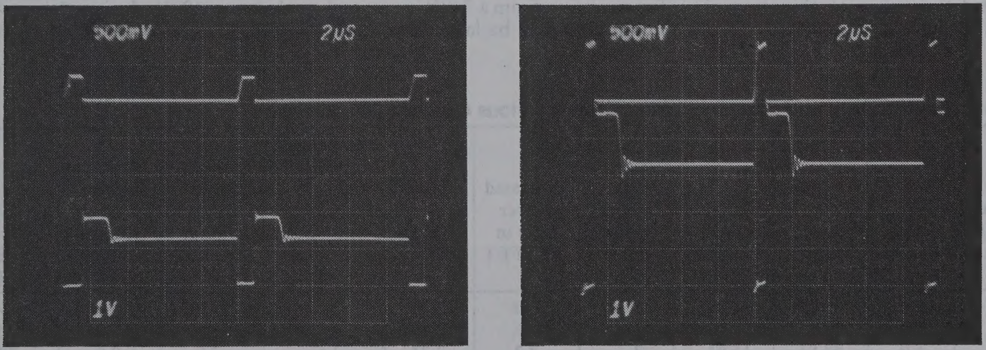
Figure 18. Oscillograms of DC Output Voltage During Step Change of Output Load Current, 85V Line Input



Output Voltage: 100mV/division
50μs/division
Step Load
Change: 10A to 20A
(a)

Output Voltage: 100mV/division
50μs/division
Step Load
Change: 20A to 10A
(b)

Figure 19. Oscillograms of DC Output Voltage During Step Change of Output Load Current, 265V Line Input



Upper Trace: Drain Current: 5A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Line Input: 85V
(a)

Upper Trace: Drain Current: 5A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Line Input: 265V
(b)

Figure 20. Oscillograms of Drain Voltage and Current with Short Circuit at Output

Attention should be paid to this point in a production design. A solution could be to add a circuit that clamps the "soft start" terminal of the control circuit to ground when the output current exceeds a predetermined level, thereby switching OFF the power supply. Resetting would be done manually once the fault condition has cleared. While this design aspect certainly needs consideration, it is of interest to see that the circuit continues to operate satisfactorily, albeit under high stress, with a short circuit output current close to 3X the rated value.

Generally, our objective has been to demonstrate the feasibility of the basic circuit concepts described, and we have not paid particular attention to design details that can be handled in a rather routine manner, according to the particular requirements of the designer. In this vein, we have taken for granted that 15V DC is available to supply the control circuit. This auxiliary DC supply could be derived from a small line frequency transformer with a rectifier and a relatively coarse voltage regulator. A 12V to 16V range of regulation would be quite satisfactory. Current consumption of the control circuit is 50mA maximum, which equates to a total power dissipation in this auxiliary power supply circuit of a little over 2W at maximum input voltage, and less than 1W at minimum input voltage.

Power Losses and Overall Efficiency

Table 3 shows the power dissipation in the various individual components of the circuit, as well as the overall efficiency, for various levels of output power, at input voltages of 90V and 260V. This data has been obtained through a combination of measurement and estimation.

The DC power delivered from the input bridge rectifier, and the DC output power, are measured directly, and the overall loss in the intervening circuitry is derived from the difference of these two measurements. The loss in the input rectifier, the HEXFET, the output rectifier, and an assumed auxiliary DC control power supply, fed from the input line through a transformer (as discussed above), are estimated individually from a knowledge of the operating voltage and currents for these components. The loss in the clamp circuit is calculated from the measured voltage across the clamp resistor; and the power loss in the output transformer and filter choke is taken as the difference between the total power dissipation, and the sum of the losses in the other components.

The overall full load efficiency arrived at in this way is 76% at 265V input, and 74% at 85V input. It should be added that an EMI filter, required in a practical system, but not included here, would reduce the overall efficiency slightly from the values shown here.

"Wide Range" Versus "Dual Range"

A point of contention may have arisen in the mind of the astute reader. This is that it is a usual design requirement to maintain rated DC output voltage during loss of the input line voltage for one cycle. In order to do this, the input reservoir capacitor, C_1 in Figure 9, must be sized to supply the required energy to the output, while its voltage must not deplete below a level at which control of the output voltage can be maintained. If this capacitor is sized to supply the required energy when operating from a 115V input, as it should be, it will then be grossly oversized for operation from a 240V input, and most likely will be larger and more expensive than the capacitance required by a conventional power supply.

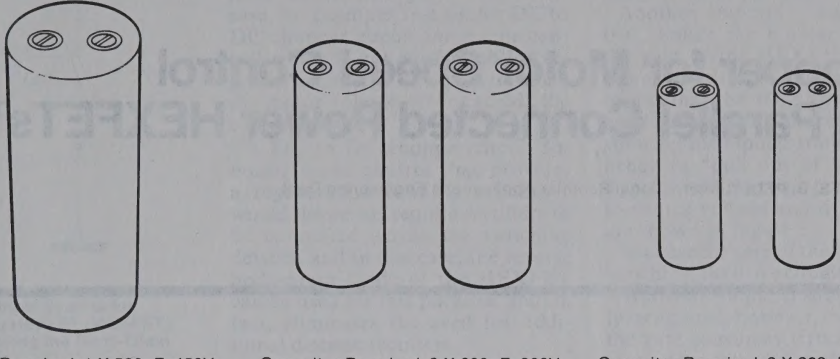
A conventional "dual voltage" power supply can operate either from 115V or 240V input, by means of switching from a voltage doubler circuit when operating at 115V, to a full rectifier bridge circuit when operating at 240V, with the two "doubler" capacitors then connected directly in series across the output of the bridge. Substantially the same primary DC source voltage is thereby maintained for both AC input voltage levels.

Taking the specific case of a 100W supply, the choice would then typically be between the single 500μF 450V capacitor, shown in Figure 21(a), for the wide range power supply, versus two 600μF 200V capacitors, shown in Figure 21(b), for the "dual voltage" supply. The single capacitor in Figure 21(a) has approximately 30% more volume than the combined volume of the two capacitors shown in Figure 20(b); the cost differential is about 11%, or $0.60 extra for the capacitor for the wide range power supply. This could be more than compensated for by the fact that the additional complication of switching from a doubler to a bridge configuration is eliminated, to say nothing of the functional convenience of not having to make any adjustments when operating from 115V or 240V input.

A quite different aspect is that if the wide regulation capability of the circuit is utilized only under the short-term condition of loss of input line voltage for one cycle, then a drastic reduction in the size of the input reservoir capacitance can be made. This is because the voltage across this capacitor can then be allowed to "drift" all the way from, say, 310V down to 120V, during the one-cycle "outage" period.

Table 3. Power Losses and Overall Efficiency Under Various Operating Conditions

Line Input Voltage V	DC Output Voltage V	Power Output W	Total Power Loss W	Estimated Power Loss in Input Rectifier W	Estimated Power Loss in HEXFET W	Power Loss in Clamp Circuit W	Estimated Power Loss in Transformer and Filter Choke W	Estimated Power Loss in Output Rectifier W	Estimated Power Loss in Control Circuit W	Overall Efficiency %
90	5.0	97.26	34.09	4	8.0	2.99	2.7	15.5	0.9	74
	5.0	73.11	24.4	3	4.6	2.60	2.4	10.9	0.9	75
	5.0	48.81	15.94	2	2.3	2.24	1.5	7.0	0.9	75
	5.0	24.40	9.3	1	0.8	2.02	1.28	3.3	0.9	72
260	5.0	96.96	30.22	1.3	5.4	2.02	3.3	15.5	2.7	76
	5.0	72.81	22.74	1.0	3.7	1.54	2.9	10.9	2.7	76
	5.0	48.66	16.69	0.7	2.3	1.29	2.7	7.0	2.7	74
	5.0	24.35	10.98	0.4	1.1	1.18	2.3	3.3	2.7	69



Capacitor required for wide range power supply when designed to operate from 115V and 240V inputs without modification.

Capacitor Required: 1 X 500μF, 450V
Total Volume: 14.72 cubic inch
Typical Cost: $6.50

Capacitors required for power supply with facility for switching from "voltage doubler" to bridge configurations for 115V and 240V inputs, respectively.

Capacitor Required: 2 X 600μF, 200V
Total Volume: 11.49 cubic inch
Typical Cost: $5.88

Capacitors required for wide range power supply when used with facility for switching from "voltage doubler" to bridge configurations for 115V and 240V inputs, respectively.

Capacitor Required: 2 X 200μF, 200V
Total Volume: 5.23 cubic inch
Typical Cost: $2.64

Figure 21. Input Reservoir Capacitors Required for Various Alternative Designs

With this design approach, it would be necessary to switch from a voltage doubler circuit to a bridge circuit when operating from 115V and 240V inputs, respectively, but the size of the required input capacitors would be reduced as shown in Figure 21(c). The volume of these capacitors is just under 50% of the volume of the capacitors required for a conventional "dual voltage" power supply, and the cost is approximately 45% — an absolute saving in the region of $3.00.

Conclusions

In order to get the most out of a power HEXFET, it is necessary to rethink basic concepts, and to design the circuitry to take maximum advantage of the special operating features of the device. An illustration of this basic precept is the 100kHz, 100W "universal" switching power supply described in this article. The circuit uses a single 500V-rated HEXFET to provide a regulated 5V DC output, over the entire range of line input voltage from 85V to 265V. ☐

CHAPTER 8
APPLICATION NOTE 941

A Chopper for Motor Speed Control Using Parallel Connected Power HEXFETs™

By S. CLEMENTE, B. PELLY, International Rectifier Applications Engineering Dept.

Summary

Today's MOSFETs are rated at currents as high as 28A continuous and 70A peak, at 100V. They are easily parallelable for higher current operation, and are attractive candidates for controlling the speed of electric motors at currents up to several hundred amperes.

This application note demonstrates an experimental DC to DC chopper circuit using parallel connected power MOSFETs, for speed control of a separately excited DC motor. The circuit operates from a 48V battery, and provides "two-quadrant" operation, with maximum motoring and regenerating currents of 200A and 140A, respectively.

Introduction

Efficient speed control of DC motors operating from DC supplies is today accomplished with switching chopper circuits using forced commutated thyristors or bipolar transistors. Battery operated systems rated at hundreds of amperes are in common use in forklift truck and electrical vehicle controllers. Larger thyristor choppers rated at thousands of amperes, at DC voltages up to 1500V, are in use in high power railway traction applications.

An exciting new power semiconductor switching device is the power MOSFET. This offers the advantage of very high gain, very rugged performance, and very fast switching speed. The power MOSFET lends itself readily to paralleling (providing the proper precautions are observed), and a power MOSFET chopper operating at currents of several hundred amperes is technically within grasp.

In this application note, we demonstrate the technical feasibility of a chopper circuit using parallel connected HEXFETs to provide a 200A, 48V output for motor speed control. A particular feature of the circuit is its facility for providing electrical braking of the motor by feeding electrical energy back to the DC source. This is accomplished through the use of the integral body-drain diode of the HEXFET, which acts as a circuit component in its own right, and provides the "freewheeling" and "flyback" functions for the "motoring" and "regenerating" modes.

The Power HEXFET

The HEXFET is a power MOSFET that is characterized by very high gain, rugged safe operating area, and fast switching speed. The basic structure is illustrated in Figure 1, and the electrical symbol is shown in Figure 2. Current flows from the drain region vertically through the silicon, then horizontally through the channel, then vertically out through the source.

The HEXFET design is based upon vertical D-MOS technology. The closed hexagonal cellular structure with the buried silicon gate allow for optimum utilization of silicon, and yield a rugged, highly reliable device.

A feature of the HEXFET (actually, of all power MOSFETs) is that it inherently has built into it an integral reverse "body-drain" diode. The full electrical symbol for the power

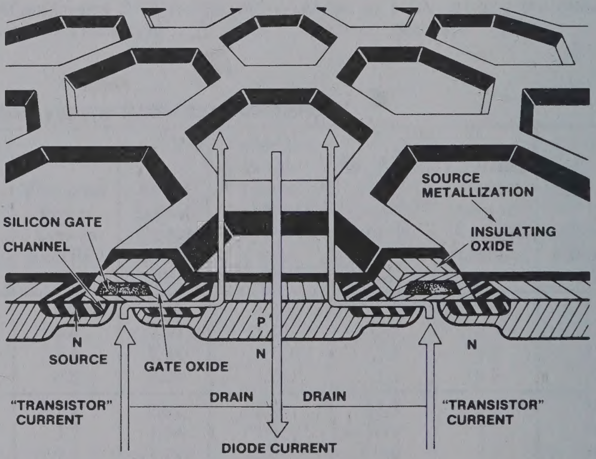


Figure 1. Basic HEXFET Structure

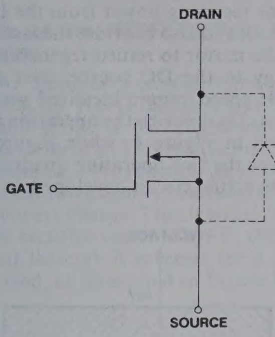


Figure 2. Electrical Symbol for Power HEXFET (MOSFET) including the Body-Drain Diode

MOSFET includes the reverse parallel rectifier shown dashed in Figure 2. The existence of this integral reverse rectifier is explained by reference to Figure 1. Current is free to flow through the middle of each source cell across a forward-biased P-N junction, and out of the drain. The path for this "reverse" current flow is at least comparable in cross-section to that of the "forward" current "transistor" channel. Far from being an inconsequential "parasitic" component, the integral reverse body-drain diode is therefore a real circuit element, with a current handling capability as high as that of the transistor.

The integral reverse body-drain diode may or may not be important in a practical circuit. In some circuits, it is irrelevant, because the circuit operation is such that the voltage across the switching device never changes polarity, and the forward conduction characteristic of the body-drain diode never comes into play. This is the case, for example, in a simple DC to DC chopper circuit for motor control which is not configured for regenerative energy flow, and in which the motor voltage never exceeds the source voltage.

A DC to DC chopper circuit for motor speed control that provides a regenerative braking capability would, however, require rectifiers to be connected across the switching devices, and in this case, the reverse body-drain diode of the HEXFET can be used for this purpose, and, in fact, eliminates the need for additional discrete rectifiers.

Potential Advantages of Power HEXFETs for Motor Drives

The power HEXFET has several unique features which make it a potentially attractive switching component for a chopper drive. These features are briefly discussed below:

High Gain

The HEXFET is a voltage driven device. The gate is isolated electrically from the source by a layer of silicon oxide. The gate draws only minute leakage current, in the order of nanoamperes, and the DC gain — in the conventional sense used for a bipolar transistor — is extremely high, typically in the order of 10^9. Actually, the gain defined in this way is rather meaningless. A more useful parameter is the transconductance. This is the change of drain current brought about by a 1V change of voltage on the gate. The transconductance of the IRF150 HEXFET is typically 10 amps per volt.

Another important advantage is that, unlike the bipolar transistor, the gain of the HEXFET does not decrease with increasing current. This means that the HEXFET is able to handle high peak current, without showing the bipolar transistor's tendency to "pull out of saturation." Typical relationships between gate-to-source voltage and drain current are shown in Figure 3.

Because the gain of the HEXFET is very high, the drive circuitry required is relatively simple. It should be clearly recognized, however, that although the gate consumes virtually no current under "steady" conditions, this is not so under transitional switching conditions. The gate-to-source and gate-to-drain self-capacitances must be charged and discharged appropriately to obtain the desired switching speed, and the drive circuit must have a sufficiently low output impedance to supply the required charging and discharging current. Even once these requirements have been catered for, the fact remains that the drive circuitry required for a HEXFET is considerably simpler than that required for a bipolar transistor.

Ruggedness

One of the outstanding features of the HEXFET is that it does not display the second breakdown phenomenon of the bipolar transistor, and

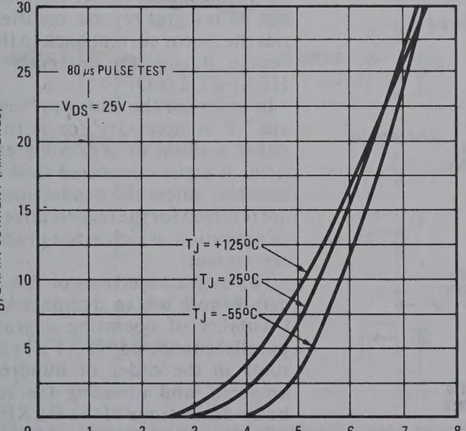


Figure 3. Transfer Characteristics IRF150

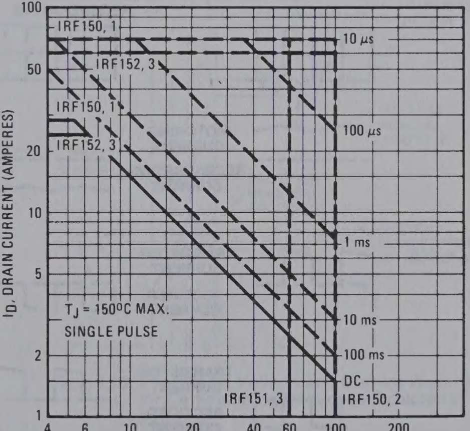


Figure 4. Maximum Safe Operating Area IRF150

as a result, it has an extremely rugged switching performance.

A simple physical explanation accounts for this superiority. If localized, potentially destructive heating occurs within a HEXFET, the carrier mobility in that area decreases. As a result, the device has a positive temperature coefficient and acts in a self-protective manner by forcing currents to be uniformly distributed throughout the silicon. The safe operating area of the IRF150 HEXFET is shown as an example in Figure 4. Note that the safe operating area for 10μs is fully rectangular; this means, in principle, that it is possible to switch 70A at 100V in this device. As a matter of good design practice, of course, one would not operate at this limit.

The absence of second breakdown means that the power HEXFET is extremely rugged which, of course, is important for this type of application.

Ease of Paralleling

Power HEXFETs are, in principle, easy to parallel, because the positive temperature coefficient forces current sharing among parallel devices. They therefore lend themselves well to the construction of a chopper rated at several hundred amperes, and the problems of paralleling will be much less than those associated with bipolar transistors.

A Basic HEXFET Two-Quadrant Chopper Circuit

Figure 5 shows the basic circuit of a DC to DC chopper that provides continuous speed control in the "motoring" mode of operation (i.e., with the motor receiving power from the DC source), and also provides the facility for the motor to return regenerative energy to the DC source, over the whole speed range. Idealized waveforms that describe the operation are shown in Figure 6, while Figure 7 defines the two operating quadrants of the actual circuit developed.

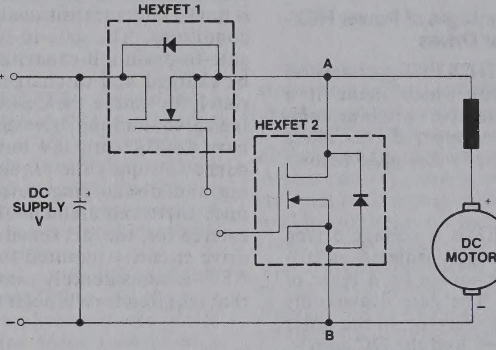


Figure 5. Basic Two Quadrant Chopper Circuit Using HEXFETs

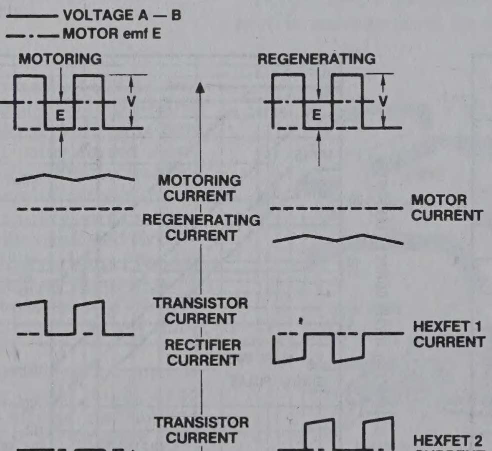


Figure 6. Idealized Operating Waveforms for Figure 5

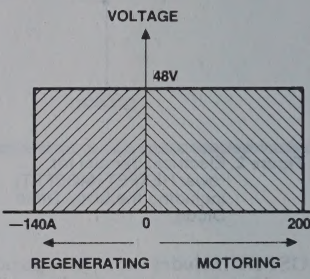


Figure 7. Motoring and Regenerating Operating Quadrants for the Circuit of Figure 5

In the "motoring" mode of operation, HEXFET 1 is switched ON and OFF, at an appropriate repetition rate, and provides control of the average voltage applied to the motor. HEXFET 2 is OFF, but its integral reverse body-drain diode acts as the conventional freewheeling rectifier and carries the freewheeling motor current during the periods when HEXFET 1 is OFF. When the motor is required to act as a generator and return energy to the DC source, HEXFET 2 is chopped ON and OFF, and controls the current fed back from the motor to the supply. In this operating mode, HEXFET 1 is OFF, but its integral reverse rectifier carries the motor current back to the DC source during the intervals when HEXFET 2 is OFF.

In order for the motor to "regenerate," it is necessary for it to have either a shunt or separately excited field. A series-connected field is not feasible, unless the connections to it are reversed for the regenerative mode of operation, which is not practically convenient.

The major objectives of this application note are to demonstrate the feasibility of operating a group of parallel connected HEXFETs at currents in the order of hundreds of amperes, and of using the reverse body-drain diode of the HEXFET as a circuit element in its own right, in the basic two quadrant chopper circuits shown in Figure 5.

To achieve these objectives, it is necessary to consider certain detailed aspects of the operation of the HEXFETs. We do this in the following section.

Use of the HEXFET's Body-Drain Diode

An important consideration when using the HEXFET's integral body-drain diode is its reverse recovery characteristic. This rectifier is a conventional P-N junction device, and therefore it exhibits a classical reverse recovery charge. That is to say, when the rectifier switches OFF, the current through it reverses for a short period, as illustrated in Figure 8.

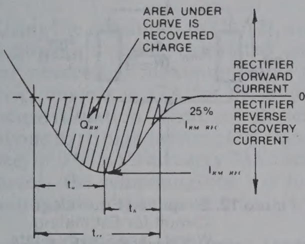


Figure 8. Rectifier Reverse Recovery

The reverse recovery time depends upon the operating conditions. For the IRF150 HEXFET, rated 28A continuous at 100V (the type used here), the reverse recovery time is about 400ns at maximum operating temperature, and about 260ns at 25° C, for an initial peak forward current of 70A, and a di/dt of 100A/μs.

Reverse recovery presents a potential problem when switching any rectifier OFF. The slower the rectifier, the greater the problem. Although the HEXFET's body-drain diode is relatively fast — not as fast as the fastest discrete rectifiers available, but considerably faster than comparably rated general purpose rectifiers — by comparison with the HEXFET itself, it is rather slow. This presents a potential problem in a chopper circuit, as we will now see.

To illustrate the problem, we will consider the motoring mode of operation. The operating condition that is troublesome is when freewheeling current is commutated from the body-drain diode of HEXFET 2 to the transistor of HEXFET 1. The operating sequence is depicted in Figure 9; the theoretical operating waveforms are shown in Figure 10.

Throughout the commutating sequence which, of course, is short by comparison with the overall fundamental operating cycle of the circuit, a constant current, I_M, is assumed to flow through the motor. During the operating period, t_0, the current, I_M, is freewheeling through the rectifier of HEXFET 2. At the start of the operating period, t_1, HEXFET 1 is turned ON, and the load current starts to transfer to the transistor of HEXFET 1. The current, i_1, in HEXFET 1 increases, while the current, i_2, flowing in the rectifier of HEXFET 2 decreases. The sum of i_1 and i_2 is equal to I_M. At the end of period t_1, the current flowing in HEXFET 1 is equal to the motor current, I_M, and the current flowing in the rectifier of HEXFET 2 is instantaneously zero.

Note that during period t_1 (also during the subsequent period t_a), the voltage across HEXFET 1 theoretically is virtually the full source voltage. This is because, as long as the rectifier of HEXFET 2 remains conducting, the voltage across it can be only its conduction voltage; the difference between this relatively small voltage and the total source voltage is developed across HEXFET 1.

This ignores the effect of circuit inductance. In practice, some of the source voltage will be dropped across circuit inductance, and the voltage across HEXFET 1 will be less than the source voltage, by the voltage drop across this inductance. A typical voltage across HEXFET 1 that takes account of the voltage drop across circuit inductance is represented by the dashed wave in Figure 10.

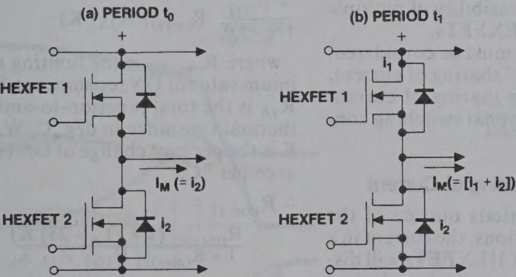


Figure 9. Commutation of Freewheeling Current I_M from the Rectifier of HEXFET 2 to the Transistor of HEXFET 1. HEXFET 1 and HEXFET 2 form a Tandem Series Connected Pair across a DC source.

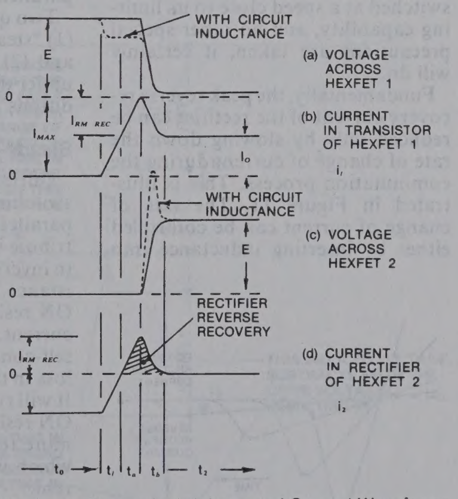


Figure 10. Theoretical Voltage and Current Waveforms for Commutating Sequence Depicted in Figure 9.

If the rectifier was "perfect," with no recovered charge, the commutation process would be complete at the end of period t_1. In practice, the rectifier current reverses during the recovery periods t_a and t_b. During the period t_a, the reverse current i_2 increases until it reaches its peak value, $I_{RM(rec)}$. The current, i_1, through HEXFET 1 is now the sum of the rectifier reverse current, i_2, and the motor current, I_M, and its peak value, I_{MAX}, is the sum of I_M and $I_{RM(rec)}$. The voltage across HEXFET 1 still theoretically remains high, because the voltage across the rectifier of HEXFET 2 is still relatively low.

During the second part of the recovery period t_b, the rectifier of HEXFET 2 begins to support reverse voltage. The rectifier recovery current i_2 decreases, and the voltage across HEXFET 1 falls to its final conduction level. Note the effect that circuit inductance has in producing an overvoltage transient across the rectifier, as illustrated by the dashed wave in Figure 10.

Certain important points are evident. First, t_1, t_a, and to a lesser extent, t_b, are high dissipation periods. Second, the peak current in HEXFET 1 is the sum of the motor current and the rectifier reverse recovery current, and this peak current occurs at an instant when the voltage across the HEXFET is high. It is important that this peak current does not violate the HEXFET's I_{DM} rating. In fact, if the HEXFET is switched at a speed close to its limiting capability, and no other special precautions are taken, it certainly will do.

Fundamentally, the peak reverse recovery current of the rectifier can be reduced only by slowing down the rate of change of current during the commutation process. This is illustrated in Figure 11. The rate of change of current can be controlled either by inserting inductance into the circuit, or by purposefully slowing down the rate-of-rise of the gate pulse that drives HEXFET 1. A linear inductor inserted in the circuit for the purpose of slowing down the rate of change of current when the HEXFET is switched ON is not attractive, because it produces a transient voltage spike when switching OFF, to say nothing of the fact that it is an added "power circuit" component.

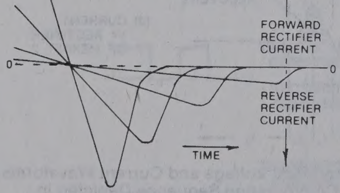


Figure 11. Reducing the Peak Rectifier Reverse Current by Reducing the Rate of Change of Current

The better practical solution is simply to slow down the switching-ON of the HEXFET by slowing down the drive signal. The peak current carried by the HEXFET can be reduced to almost any desired extent, at the expense of prolonging the high dissipation period. This is a necessary compromise in order to keep the peak current within safe limits, and as a practical matter, the switching losses, when averaged over the full operating cycle, are relatively small, for the operating frequencies that will be of interest in this application (normally a few hundred to a few thousand Hz).

Note that it is not necessary (nor desirable) to slow the switching-OFF; hence, the energy dissipation at switch-OFF will be relatively small by comparison with that at switch-ON.

Paralleling of HEXFETs

A key question that is fundamental to the successful demonstration of a chopper operating at hundreds of amperes, is the feasibility of multiple paralleling of HEXFETs.

Two questions must be considered: (1) "steady-state" sharing of current, and (2) dynamic sharing of current under the transitional switching conditions.

Steady-State Sharing of Current

During the periods outside of the switching transitions, the current in a parallel group of HEXFETs will distribute itself in the individual devices in inverse proportion to their ON resistance. The device with the lowest ON resistance will carry the highest current. This will, to an extent, be self-compensating, because the power loss in this device will be the highest. It will run hottest, and the increase in ON resistance due to heating will be more than that of the other devices, which will tend to equalize the current.

An analysis of the "worst case" device current in a group of "N" parallel connected devices can be based on the simplifying assumption that (N - 1) devices have the highest limiting value of ON resistance, while just one lone device has the lowest limiting value of ON resistance. The analysis can then be concentrated on the current in this one device.

The equivalent electrical circuit shown in Figure 12 simplifies the analysis further by assuming the number of devices is sufficiently large that the current that flows through each of the high resistance devices is approximately $I_{TOT}/^{(N-1)}$. On this assumption, the voltage drop across the lone low resistance device, and hence the current in it, can be calculated.

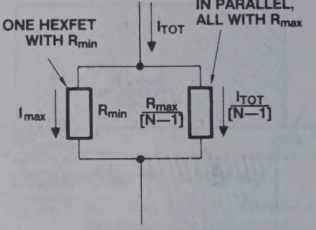


Figure 12. Simplified Equivalent Circuit for Estimating Worst Case Steady-State Current Unbalance

The ON resistance of each of the "high resistance" devices, at operating temperature, T, is given by:

$$R_{(max)T} = R_{(max)25}\ (1 + [(T_A - 25) + \frac{I^2_{TOT}}{(N-1)^2}\ R_{(max)T}\ R_{JA}]\ K)$$

where $R_{(max)25}$ is the limiting maximum value of ON resistance at 25° C, R_{JA} is the total junction-to-ambient thermal resistance in deg. C/W, and K is the per unit change of ON resistance per °C.

$$\therefore R_{(max)T} = \frac{R_{(max)25}\ (1 + [T_A - 25]\ K)}{1 - R_{(max)25}\ \frac{I^2_{TOT}}{(N-1)^2}\ R_{JA}\ K} \qquad (1)$$

The voltage drop, V, across the parallel group is:

$$V = \frac{I_{TOT}}{(N - 1)} \cdot R_{(max)T} \qquad (2)$$

The resistance of the one low resistance device at its operating temperature is:

$$R_{(min)T} = R_{(min)25}\ (1 + [T_A - 25) + V I_{(max)}\ R_{JA}]\ K)$$

where $R_{(min)25}$ is the limiting minimum value of ON resistance at 25° C, and $I_{(max)}$ is the current in this device.

$$\text{But, } R_{(min)T} = \frac{V}{I_{(max)}}$$

$$\therefore I_{(max)} = \frac{-b + \sqrt{(b^2 + 4aV)}}{2a} \qquad (3)$$

where:

$b = R_{(min)25} (1 + [T_A - 25] K)$

$a = R_{(min)25} V R_{JA} K$

The following example shows the "worst case" degree of current sharing that can be expected, by applying the above relationships to the IRF150 HEXFET, and making the following assumptions:

$R_{(max)25} = 0.045\Omega$

$R_{(min)25} = 0.03\Omega$

$R_{JA} = 3$ deg. C/W

$\frac{I_{TOT}}{(N - 1)} = 20A$

$K = 0.006$ per degree C

$T_A = 35°C$

Using the relationships (1), (2), and (3) above, it can be calculated that the "worst case" maximum value of device current is 27A for the hypothetical situation where all devices but one have high limiting ON resistance, of 0.045Ω, and carry 20A each, whereas the remaining one has low limiting ON resistance of 0.03Ω.

Dynamic Sharing of Current Under Switching Conditions

Turn-On

It is necessary to take positive steps to ensure that the current is distributed properly between a group of parallel connected devices during the switching transition. Since the HEXFETs will not all have identical threshold and gain characteristics, some will tend to switch sooner than others, and attempt to take more than their share of the current. Adding to the problem is the fact that circuit inductance associated with each device may be different, and this will also contribute to unbalancing the current under switching conditions.

The problem will be introduced by considering the switching waveforms for the basic chopper circuit, shown in Figure 5, which contains a single HEXFET in each of the "motoring" and "regenerating" positions. We will consider the motoring mode of operation, under which HEXFET 1 is switched ON and OFF, while the motor current (assumed to be smooth, due to the motor inductance) alternates between this HEXFET and the body-drain diode of HEXFET 2, which acts as a freewheeling rectifier.

Figure 13 shows waveforms of drain current, drain-to-source voltage, and gate voltage during the turn-ON interval. We have already seen that in order to limit the peak recovery current of the body-drain diode of HEXFET 2, the gate drive voltage for HEXFET 1 must be applied at a controlled rate. This is the reason that the applied drive pulse is shown increasing at a relatively slow rate.

At time, t_0, the drive pulse starts its rise. At t_1, it reaches the threshold voltage of the HEXFET, and the drain current starts to increase. At this point, two things happen which make the gate-source voltage waveform deviate from its original "path." First, inductance in series with the source which is common to the gate circuit develops an induced voltage, as a result of the increasing source current. This voltage counteracts the applied gate drive voltage and slows down the rate-of-rise of voltage appearing directly across the gate and source terminals; this, in turn, slows down the rate-of-rise of the source current. This is a negative feedback effect; increasing current in the source produces a counteractive voltage at the gate, which tends to resist the change of current.

The second factor that influences the gate-source voltage is the so-called "Miller" effect. During the period t_1 to t_2, some voltage is dropped across circuit inductance in series with the drain, and the drain-source voltage starts to fall. The decreasing drain-source voltage is reflected across the drain-gate capacitance, pulling a discharge current through it, and increasing the effective capacitance load on the drive circuit. This, in turn, increases the voltage drop across the impedance of the drive circuit and decreases the rate-of-rise of voltage appearing between the gate and source terminals. This also is a negative feedback effect;

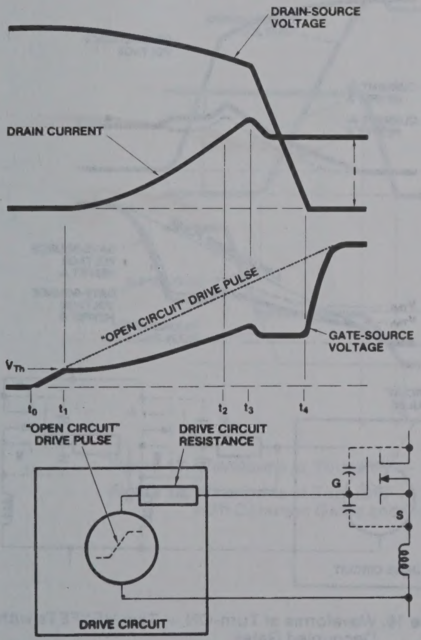


Figure 13. Waveforms at Turn-ON — Single HEXFET

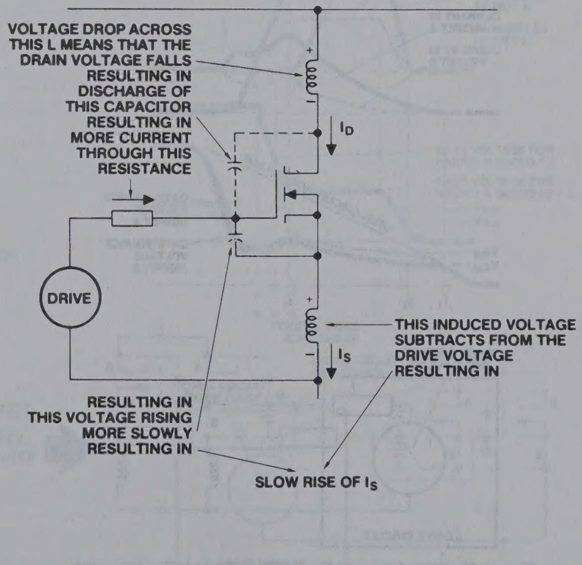

VOLTAGE DROP ACROSS THIS L MEANS THAT THE DRAIN VOLTAGE FALLS RESULTING IN DISCHARGE OF THIS CAPACITOR RESULTING IN MORE CURRENT THROUGH THIS RESISTANCE
I_D
DRIVE
THIS INDUCED VOLTAGE SUBTRACTS FROM THE DRIVE VOLTAGE RESULTING IN
I_S
RESULTING IN THIS VOLTAGE RISING MORE SLOWLY RESULTING IN
SLOW RISE OF I_S

Figure 14. Diagrammatic Representation of Effects When Switching-ON

increasing current in the drain results in a fall of drain-to-source voltage, which, in turn, slows down the rise of gate-source voltage and tends to resist the increase of drain current. These effects are illustrated diagrammatically in Figure 14.

This state of affairs continues throughout the period t_1 to t_2, while the current in the HEXFET rises to the level of the current, I_M, already flowing in the freewheeling rectifier, and it continues into the next period, t_2 to t_3, while the current increases further, due to the reverse recovery of the freewheeling rectifier.

At time t_3, the freewheeling rectifier starts to support voltage, while the drain current and the drain voltage start to fall. The rate-of-fall of drain voltage is now governed by the Miller effect, and an equilibrium condition is reached, under which the drain voltage falls at just the rate necessary for the voltage between gate and source terminals to satisfy the level of drain current established by the load. This is why the gate-to-source voltage falls as the recovery current of the freewheeling rectifier falls, then stays constant at a level corresponding to the motor current, while the drain voltage is falling.

Finally, at time t_4, the HEXFET is switched fully ON, and the gate-to-source voltage rises rapidly towards the applied "open circuit" value.

The gate-to-source voltage waveform for the circuit shown in Figure 5, with just a single device in each position, provides the clue to the difficulties that can be expected with parallel connected devices. The first potential difficulty is that if we apply a common drive signal to all gates in a parallel group, then the first device to turn ON — the one with the lowest threshold voltage — will tend to slow the rise of voltage on the gates of the others, and further delay the turn-ON of these devices. This will be due to the Miller effect. The inductive feedback effect, on the other hand, only influences the gate voltage of its own device (assuming that each source has its own separate inductance).

The second potential difficulty is that if the individual source inductances are unequal, then this will result in dynamic unbalance of current, even if the devices themselves are perfectly matched. Obviously, the solution to this is to ensure that inductances associated with the individual devices are as nearly equal as possible. This can be done by proper attention to the circuit layout.

Figure 15 illustrates the turn-ON of two parallel connected HEXFETs, A and B, having different threshold voltages, V_{thA} and V_{thB}, with their gates connected directly together. V_{thB} is greater than V_{thA}, and HEXFET A switches ON first, at time t_1. The voltage between gate and source of HEXFET B is now "deflected" slightly as shown, due to the Miller effect, and the turn-ON of HEXFET B is delayed until time t_2. During the period t_2 to t_3, the gate-source voltages "drift" towards one another (being kept apart only by the individual source inductances), and this produces a drifting apart of the drain currents, with a significant resulting unbalance.

This basic problem stems from the fact that the two gates are coupled together by the common impedance of the drive source. If, on the other hand, the drive circuit is designed to have a low output impedance, and the gates are decoupled from one another by individual gate resistors, the dynamic unbalance can be alleviated.

Figure 16 illustrates theoretical waveforms for two parallel connected HEXFETs, A and B, having different threshold voltages, V_{thA} and V_{thB}, as assumed in Figure 14, driven from a low impedance circuit with individual gate resistors. The dynamic unbalance of currents in the two HEXFETs is now substantially reduced.

In summary, attention must be paid to the following points, in order to ensure satisfactory sharing of current between parallel HEXFETs at turn-ON:

- Threshold voltages should be within determined limits.

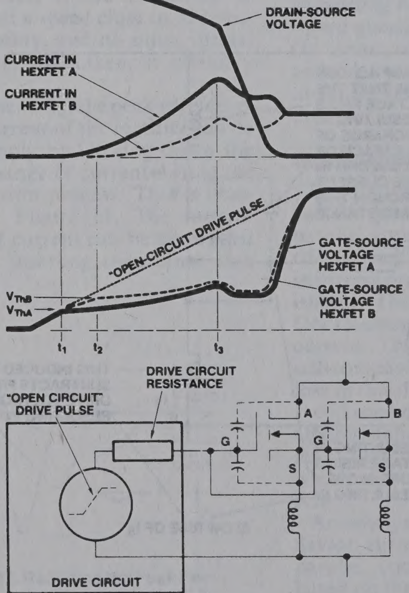


Figure 15. Waveforms at Turn-ON — Two HEXFETs with Gates Tied Together

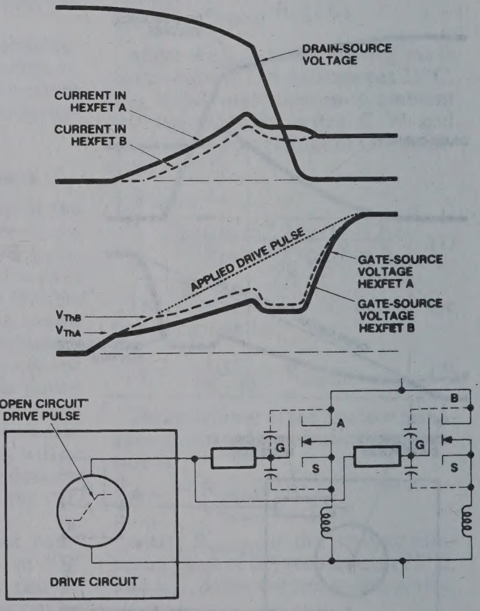


Figure 16. Waveforms at Turn-ON — Two HEXFETs with Decoupled Gates

- Inductance that is common to the gate and source circuits of the individual devices must be matched within determined limits.
- Gates should be decoupled with individual resistors, and the output impedance of the drive circuit must be low by comparison.

Turn-Off

Similar considerations apply to the dynamic sharing of current during the turn-OFF interval. Figure 17 shows theoretical waveforms for HEXFET 1 in the circuit of Figure 5 during the turn-OFF interval. At t_0, the gate drive starts to fall. At t_1, the gate voltage reaches a level that just sustains the drain current, I. The drain-to-source voltage now starts to rise. The Miller effect governs the rate-of-rise of drain voltage and holds the gate-to-source voltage at a level corresponding to the constant drain current. At t_3, the rise of drain voltage is complete, and the gate voltage starts to fall at a rate determined by the gate-source circuit impedance, while the drain current falls to zero.

Figure 18 shows theoretical waveforms for two parallel connected HEXFETs with their gates connected directly together. For purposes of discussion, the source inductance is assumed to be zero. At t_1, the gate voltage reaches the point at which HEXFET B can no longer sustain its drain current. The load current now redistributes; current in HEXFET B decreases, while that in HEXFET A increases. At t_2, HEXFET B can no longer sustain its current; both HEXFETs now operate in their "linear" region, and the drain voltage starts to rise. The gate-to-source voltage is kept practically constant by the Miller effect, while the currents in the two HEXFETs remain at their separate levels. Clearly, the unbalance of current in this example is significant.

Figure 19 shows waveforms for two HEXFETs having their gates tied directly together, but with individual inductances in series with each source. The negative feedback effect of these inductances has a pronounced balancing effect upon the individual drain currents. While the drain voltage is rising, however, the voltages on the individual gates, being "separated" only by the source inductances, drift towards one another, while the two drain currents drift apart.

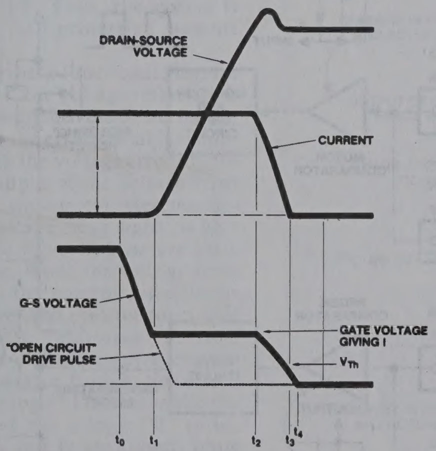
Figure 20 shows waveforms for two parallel connected HEXFETs, driven from a low impedance circuit, with their gates decoupled by individual resistors, and with inductance in series with each source. Because the gates are now separated by decoupling resistors, the gate voltages no longer drift together, and the drain currents no longer drift apart, during the period when the voltage is rising. This minimizes the unbalance of current.

In summary, to achieve good sharing of current when switching-OFF, the following points are important:

- Threshold voltage and transconductance of the HEXFETs should be within determined limits.
- Source inductance is a key factor in keeping the individual currents balanced.
- Gates should be decoupled with individual resistors. The output impedance of the drive circuit must be low.

A Complete Functional Control Scheme for a Two-Quadrant Chopper

A simplified functional diagram of the control and drive circuitry for a two-quadrant HEXFET chopper is shown in Figure 21; this is intended to demonstrate the basic operating principle of the overall chopper system, and differs in some minor details from the actual practical circuitry presented later (Figure 25).



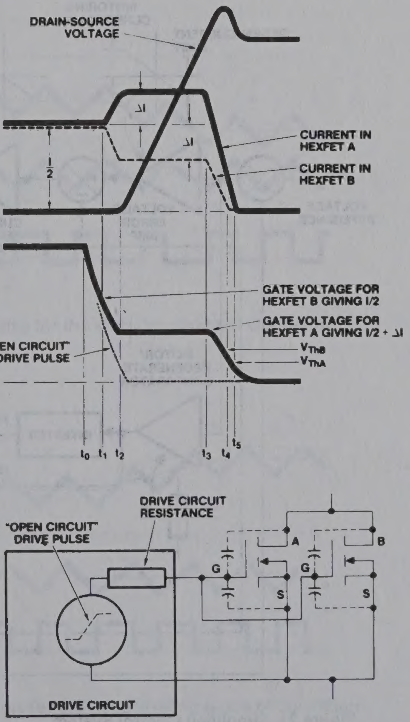


Figure 17. Waveforms at Turn-OFF — Single HEXFET

Figure 18. Waveforms at Turn-OFF — Two HEXFETs with Common Gates and Common Sources ➡

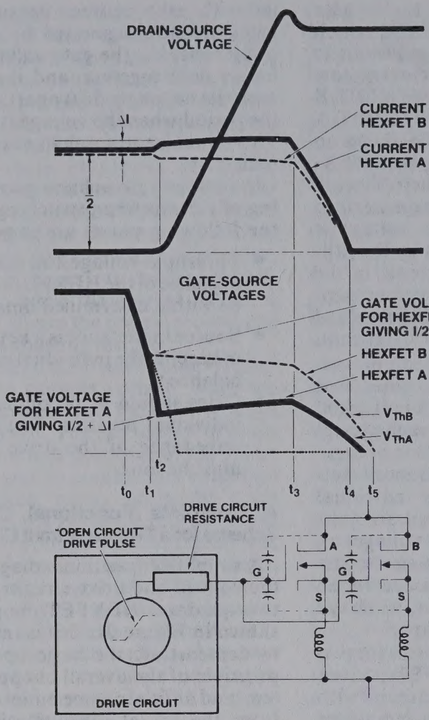


Figure 19. Waveforms at Turn-OFF — Two HEXFETs with Common Gates and Decoupled Sources

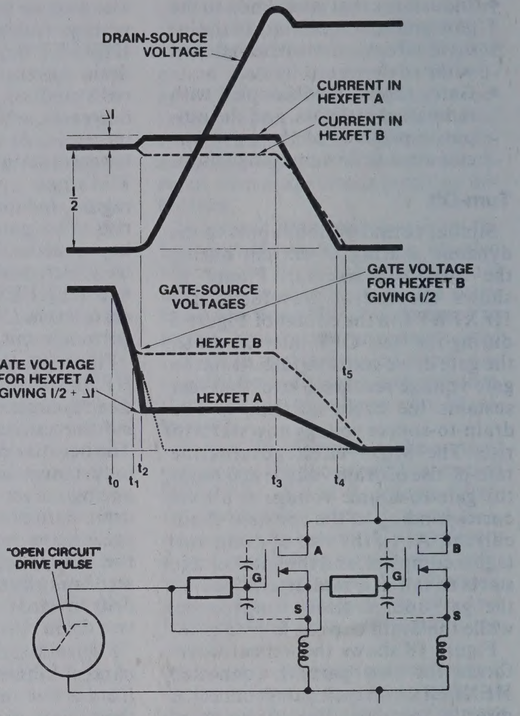


Figure 20. Waveforms at Turn-OFF — Two HEXFETs with Decoupled Gates and Decoupled Sources

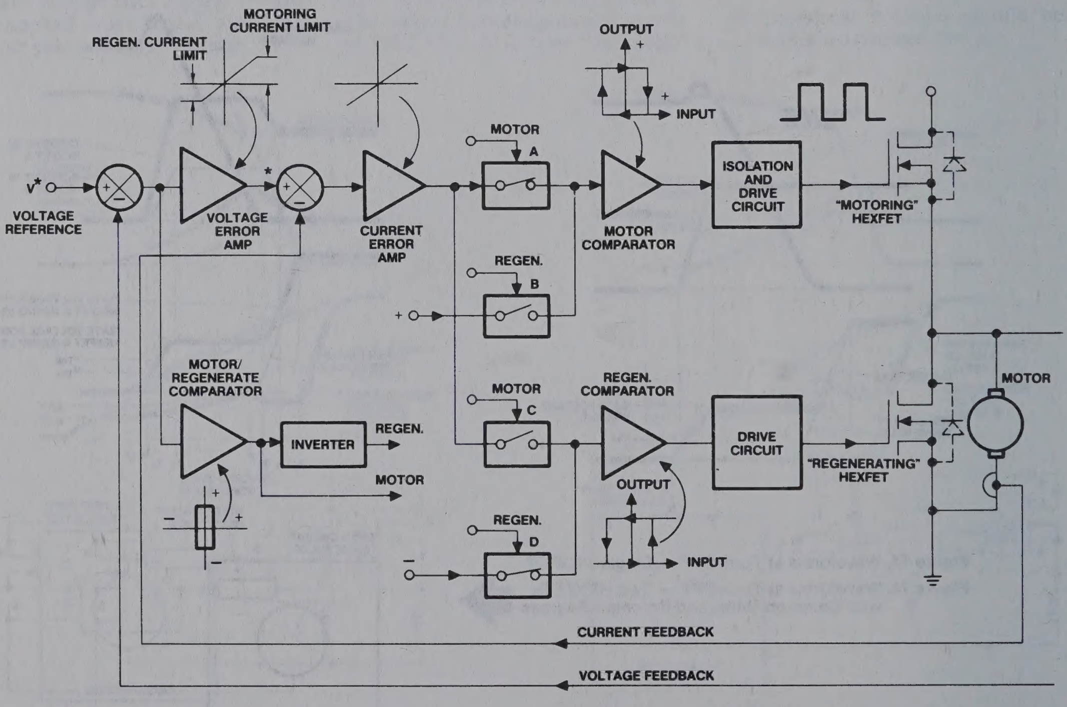


Figure 21. Simplified Control System

The control system has an outer voltage feedback loop, which compares the motor voltage with a reference voltage and processes the resulting "error" signal to keep the motor voltage essentially equal to the reference value. In a practical system, the voltage control loop could be complemented with a signal proportional to the armature voltage drop, to give a closer regulation of actual motor speed. Alternatively, the voltage feedback signal could be substituted with a signal from a tachogenerator, to give a more precise speed regulation.

An inner control loop regulates the current to the level required to satisfy the load on the motor. The current control loop also determines the chopper switching frequency by regulating the peak-to-peak ripple current between preset upper and lower limits. This it does by switching the HEXFET ON whenever the current falls a given amount below the reference value, and switching the HEXFET OFF whenever the current rises a given amount above it.

The current control loop also provides instantaneous limiting of the peak HEXFET and motor current. This is accomplished simply by setting a maximum limit on the current reference signal and clamping it to this level. Whenever the instantaneous motor current attempts to exceed the maximum current reference by more than the preset peak ripple current, the HEXFET is immediately switched OFF. Thus, the system is completely self-protecting against overcurrent.

Referring to the functional diagram in Figure 21, the voltage reference is compared with the voltage across the motor, and the error signal is amplified through the voltage error amplifier. The output of the voltage error amplifier is the current reference signal. The voltage error signal is also fed into the *motor-regenerate* logic comparator. When the voltage error is positive, the current reference is also positive, and the control circuit is demanding "motoring" current. The output of the *motor-regenerate* logic comparator is high, the *motor* signal has a logic "1" value, while the *regen* signal has a logic "0" value. Switches A and D are closed, while switches B and C are open.

When the current reference is negative, the control circuit is demanding "regenerating" current. The output of the *motor-regenerate* logic comparator is negative, the *regen* signal has a logic "1" value, while the *motor* signal has a logic "0" value. Switches B and C are closed, while A and D are open.

The *motor-regenerate* logic comparator has a built-in hysteresis to prevent unwanted "bouncing" back and forth between the "regeneration" and "motoring" modes of operation, at low current levels.

Consider the "motoring" mode of operation. The positive current reference signal is compared with a signal representing the actual motor current; the difference is amplified through the current error amplifier. The output of this amplifier is fed through switch A, which is closed, to the *motor* comparator. This comparator produces a "0" output signal in response to a positive input signal above a preset threshold level, and a "1" output signal in response to a negative input signal below a certain preset level.

The output signal of the *motor comparator* is isolated and shaped to become the gate drive signal for the "motoring" HEXFET. The "motoring" HEXFET is thereby switched ON when the motor current falls a predetermined amount below the reference and OFF whenever the motor current rises a predetermined amount above the reference value, while the switching frequency automatically adjusts itself to keep the peak-to-peak ripple current constant. The peak-to-peak ripple current and operating frequency can be adjusted by adjusting the hysteresis of the *motor* comparator.

Note that in the motoring mode, switch D is closed, applying a steady negative input to the *regen* comparator, and shutting OFF the gate drive signal to the "regenerating" HEXFET. Theoretical waveforms which illustrate the operation of this scheme in the motoring mode are illustrated in Figure 22.

In the regenerating mode of operation, switches B and C are closed. A continuous positive signal is applied to the input of the *motor* comparator, shutting OFF the drive to the "motoring" HEXFET. The current reference is negative, and the current error signal is fed to the input of the *regen* comparator. This comparator produces a "1" output signal in response to a positive input signal above a certain preset level, and a "0" output signal in response to a negative input signal below a given preset level. The "regenerating" HEXFET is now switched ON whenever the regenerative current from the motor falls a preset amount below the reference value, and OFF whenever the motor current rises a preset amount above the reference value. Theoretical waveforms which illustrate the operation in the regenerating mode are shown in Figure 23.

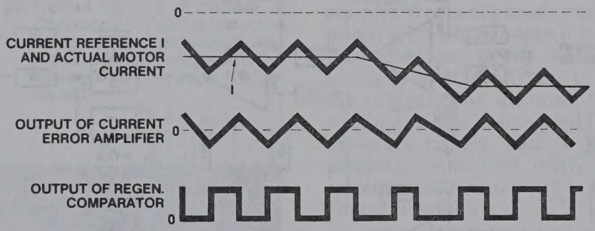

0
CURRENT REFERENCE I AND ACTUAL MOTOR CURRENT
I
OUTPUT OF CURRENT ERROR AMPLIFIER
0
OUTPUT OF REGEN. COMPARATOR
0

Figure 22. Theoretical Waveforms for the Motoring Mode of Operation

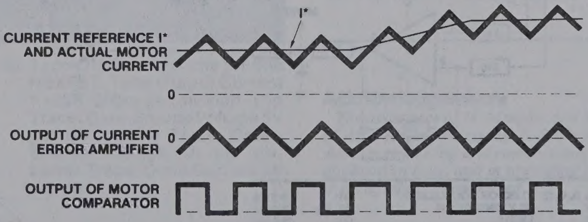

I*
CURRENT REFERENCE I* AND ACTUAL MOTOR CURRENT
0
OUTPUT OF CURRENT ERROR AMPLIFIER
0
OUTPUT OF MOTOR COMPARATOR

Figure 23. Theoretical Waveforms for the Regenerating Mode of Operation

A 48V, 200A Experimental Chopper

Power Circuit

A schematic diagram of the power circuit of an experimental laboratory chopper is shown in Figure 24. This employs a total of ten IRF150 HEXFETs connected in parallel for the "motoring" switch, and five IRF150 HEXFETs connected in parallel for the "regenerating" switch.

All HEXFETs are mounted on a 22-inch length of aluminum heatsink extrusion, with outer dimensions of 5 inches by 3 inches, with the regenerating HEXFETs being isolated electrically from the heatsink.

The assembly is capable of delivering 200A forward "motoring" current and 140A of "regenerating" current. The "motoring" HEXFETs by themselves actually are capable of carrying about 300A of output current; the 200A limit is set by the current carrying capacity of the five freewheeling body-drain diodes of the "regenerating" HEXFETs.

Individual zener diode and snubber circuits are connected across the drain-to-source terminals of each HEXFET to provide individual protection against overvoltage transients. A total of five local decoupling capacitors, each of 22μF, are distributed at intervals along the "positive" and "negative" bus bars of the assembly, to prevent unwanted oscillation of the local DC source voltage.

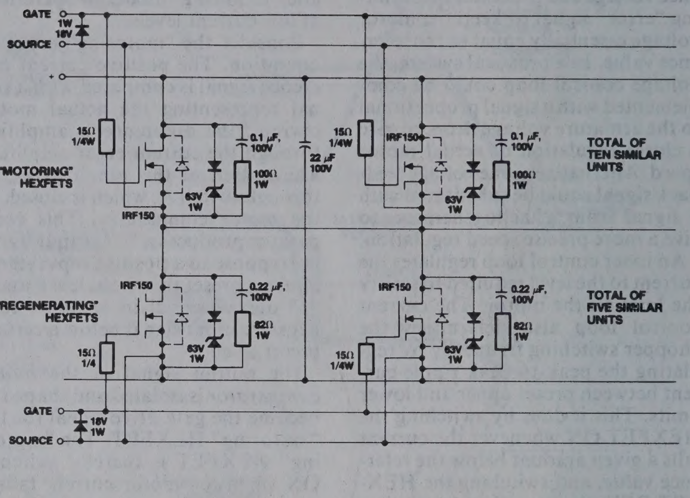
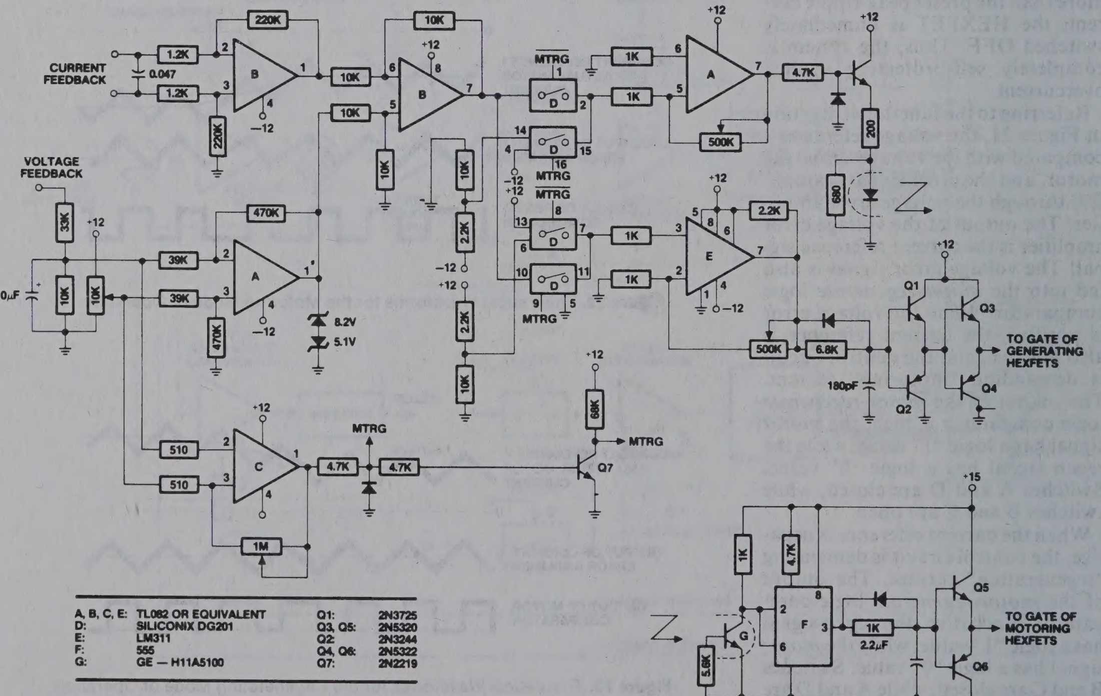


Figure 24. Power Circuit Schematic

Control and Drive Circuitry

Figure 25 shows a diagram of the control and drive circuitry. This is based upon the functional circuit shown in Figure 21 and requires no additional explanation other than to point out that for practical reasons, some of the signal polarities are opposite to those assumed for the simplified functional circuit of Figure 21.



A, B, C, E:	TL082 OR EQUIVALENT	Q1:	2N3725
D:	SILICONIX DG201	Q3, Q5:	2N5320
E:	LM311	Q2:	2N3244
F:	555	Q4, Q6:	2N5322
G:	GE — H11A5100	Q7:	2N2219

Figure 25. Control and Drive Circuit Schematic

Test Results

Practical test results are shown in Figures 26 through 30.

Figure 26 shows the current when the motor accelerates from standstill to about half speed. The current limit circuit keeps the peak motor current to just over 200A. The chopping frequency is about 2 kHz.

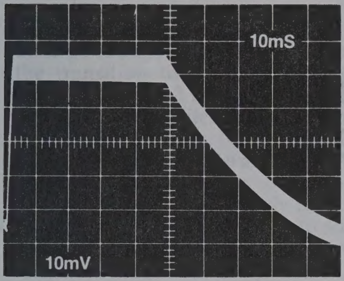


Figure 26. Motor Current under Acceleration. Peak Motor Current = 220A. 40A per division. 10ns per division.

Figure 27 shows motor current and voltage waveforms when accelerating from half speed to almost full speed, then decelerating back to half speed. The current limit holds the peak motoring current to about 205A, and the peak regenerating current to about 140A.

Figure 28 shows the output voltage and current of the chopper with a passive inductive load. Note the classical linear rise and fall of the current associated with an inductive load.

Figures 29 and 30 show turn-ON and turn-OFF oscillograms respectively for one HEXFET, with the chopper operating with a passive inductive load of 120A. These waveforms generally agree with the foregoing theoretical discussion. Note, however, in Figure 30, that the gate voltage reverses at switch-OFF; this is due to resonance between the gate capacitance and circuit inductance.

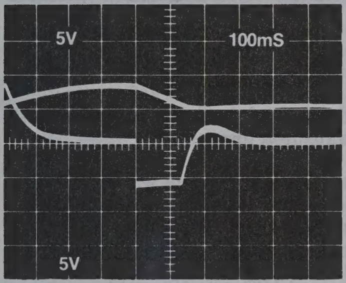


Figure 27. Motor Voltage & Current when Accelerating & Decelerating. Peak Motoring Current = 205A. Peak Regenerating Current = 140A. Top Trace: Voltage 25V per division. Bottom Trace: Current 115A per division.

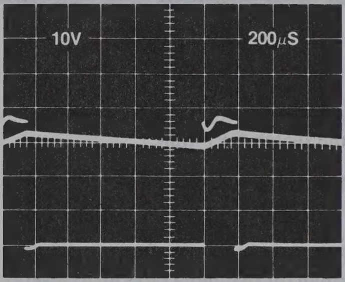


Figure 28. Output Voltage & Current of Chopper into Passive Inductive Load — 220 μs per division. Top Trace: Current 40A per division. Lower Trace: Voltage 10V per division.

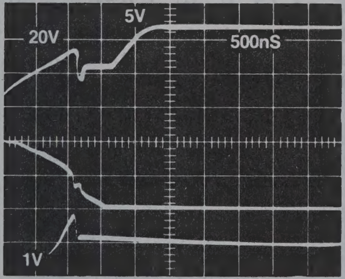


Figure 29. Turn-On Oscillograms for one HEXFET. Total Output Current = 120A. 500ns per division. Top Trace: Gate-Source Voltage 5V per div. Middle Trace: Drain-Source Voltage 20V per div. Lower Trace: Drain Current 10A per div.

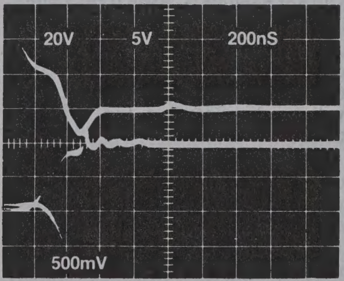


Figure 30. Turn-Off Oscillograms for one HEXFET. Total Output Current = 120A. 200ns per division. Top Trace: Gate-Source Voltage 5V per div. Middle Trace: Drain-Source Voltage 5A per div. Lower Trace: Drain Current 5A per div.

Conclusions

This application note has demonstrated the technical feasibility of a DC-to-DC chopper using parallel connected HEXFETs for motor speed control, operating at the 200A level, and the use of the HEXFET's body-drain diode to provide the freewheeling and flyback functions needed for two quadrant operation. The potential attractions of using HEXFETs are simplicity of drive circuitry, ruggedness, speed of response, ease of paralleling and overall compactness.

Power HEXFETs also offer an interesting system advantage in this type of application. Due to the ease of operating at high frequency, a separately excited field winding, with the added motor controlability and superior system performance that this provides, becomes a practical reality. Present-day choppers using bipolar transistors or thyristors generally operate at relatively low frequency (in order to keep them simple), and require a series-connected field winding to keep the motor ripple current to an acceptable level. With the higher chopper frequency made possible by power HEXFETs, on the other hand, the inductance of the motor armature is by itself insufficient to smooth the current, thus allowing the field winding to be disassociated from the armature circuit, and to be independently controlled, offering better system performance and superior control flexibility.

As improvements in circuit design, MOSFET technology, packaging, and device costs all take place, the type of system described in this application note will become economically as well as technically superior to today's chopper systems using bipolar transistors or thyristors. ☐

Acknowledgements

The assistance of H. Murphy and T. Gilmore of Allis Chalmers, and of F. Stich of Siemens Allis, in reviewing and commenting upon this application note, and in providing the motor, is gratefully acknowledged.

CHAPTER 9

APPLICATION NOTE 942

Simplified HEXFET™ Power Dissipation and Junction Temperature Calculation Speeds Heatsink Design

by R. SEVERNS, International Rectifier Applications Engineering Department

The reliability and life expectancy of HEXFETs, like that of any power semiconductor, is directly related to the maximum junction temperature the device experiences. It is, therefore, vital for the designer to be able to accurately determine the device power dissipation and the maximum junction temperature. The power dissipation and maximum junction temperature along with the ambient temperature, determine the design of the heatsink.

The first step in this process is to determine the total power dissipation in the device. This is not trivial since while the power dissipation determines the junction temperature, the power dissipation is itself a function of the junction temperature, because the on-resistance increases with temperature. Because of the nonlinear nature of the on-resistance increase, which varies from one device type to another, strictly analytical solutions can be time-consuming.

This application note presents a simple graphical method for determining the total power dissipation and junction temperature for any given heatsink. The method provides a graphic illustration of the conditions that provide a sound and stable thermal design, as well as showing the designer conditions that are to be avoided because they lead to unnecessary thermal runaway.

The total power dissipation (P_T) is the sum of the switching transition loss (P_S), the conduction loss (P_C), a fraction of the gate drive power (P_G), and the loss due to I_{DSS} (P_L), during the switch OFF time.

Switching Transition Loss

Because of the rapid transition times which are possible, P_S for a HEXFET can, in theory, be almost arbitrarily small for switching rates up to several hundred kHz if a sufficiently low impedance gate driver is used. In a practical circuit, however, there are often limitations on the switch transition time, due to transient ringing of parasitic circuits or the capabilities of the rectifier diodes, so that P_S is usually not negligible. Even if the switching time were zero, any practical circuit will have stray capacity in the drain circuit. The energy stored in this capacity while the device is OFF will be dissipated in the switch at turn-on.

Unlike a bipolar switch, the losses during switching for a MOSFET are not increased by quasi-saturation or current tailing. As shown in Figure 1(a), the switching waveforms for an inductive load can usually be closely approximated by two straight lines. The switching loss for each type of transition (turn-on or turn-off) is then:

$$P_S = \frac{(V_{DS(max)} \cdot I_{D(max)})}{2}\,\tau_s f_s \qquad (1)$$

where f_s is the switching frequency.

The values for $V_{DS(max)}$ and τ_s will probably differ for the turn-on and turn-off transitions due to stray inductance and capacitance. P_S is then the sum of the turn-on and turn-off transition losses.

If the load is resistive, then the switching transitions will be as shown in Figure 1(b) and the losses due to each type of transition can be expressed as:

$$P_S = \frac{(V_{DS(max)} \cdot I_{D(max)})}{6}\,\tau_s f_s \qquad (2)$$

If, because of load or drive circuit peculiarities, the straight line approximations of Figure 1 are not sufficiently accurate, then the power dissipation can be found from:

$$P_S = f_s \int_0^{\tau_s} V_{DS}(t) \cdot I_D(t)\,dt \qquad (3)$$

Usually a simple piecewise linear approximation for $V_{DS}(t)$ and $I_D(t)$ is sufficient.

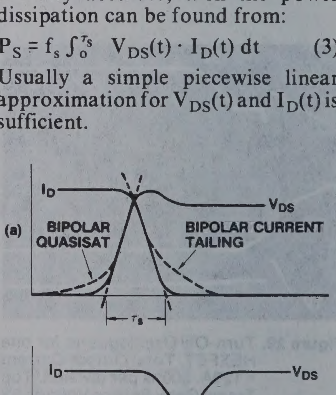


Figure 1. Inductive and Resistive Load Switching Transitions

When the switching losses are calculated from circuit oscillographs, the foregoing equations are quite accurate, but if the losses are being estimated in advance of breadboarding the circuit, a slightly different procedure is needed.

It is not unusual for $C_{DS} + C_{stray}$ to be large enough to significantly alter the transition time of V_{DS} during turn-off. Figure 2 shows an oscillograph of typical switching waveforms in a power converter. Note that even though the gate turn-on and turn-off times are identical, the transition time at turn-off is noticeably longer than at turn-on. This is due to the finite charging time for the capacitance in the drain circuit by the drain load current.

This capacitance, as shown in Figure 3, includes C_{oss} which is integral to the device, and the stray capacitance in the drain circuit. A TO-3 case, using a thin mica or plastic film insulating washer will add about 200pF to C_{stray}. A 0.062″ beryllia washer, on the other hand, will add only about 25pF to C_{stray} and as an additional benefit will provide a lower case-to-heatsink thermal impedance ($R_{\theta CH}$).

P_S can be estimated by using equations (1) or (2) with the anticipated transition times due to the gate drive characteristics in the absence of the output capacitance and then include an additional loss (P_{SC}) due to the drain capacitance.

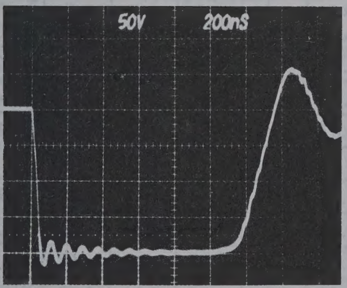


Figure 2. Effect of Drain-Source Capacity

This loss is:

$$P_{SC}=\frac{(C_{DS}+C_{stray})\,V^2_{DS}f_s}{2} \qquad (4)$$

where V_{DS} is the value of V_{DS} at switch turn-on.

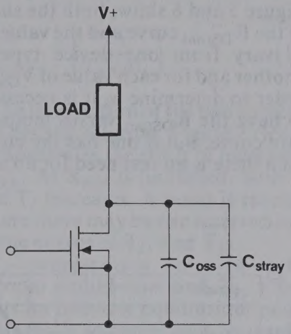


Figure 3. Drain-to-Source Capacitances

Drain-Source Leakage Current Losses

During the switch OFF period, a small temperature-dependent current (I_{DSS}) will flow through the switch.

The loss due to this current is:

$$P_L = I_{DSS} \cdot V_{DS}\,(1 - D) \qquad (5)$$

where V_{DS} is the drain-source voltage during the OFF time and D is the ON time duty cycle of the switch.

Even for T_J = 150°C, this loss is usually quite small, of the order of ½W or less in a 400V device. There are, however, circumstances where P_L is not insignificant. If due to the drive circuit, $V_{GS} > 0$ during the OFF time, then I_{DSS} can be an order of magnitude larger, and in that case, P_L may well be important. This problem can arise when driving the HEXFET from IC logic.

Normally, with the logic driver in the "0" state, the current into the driver from the HEXFET is minute (nanoamperes or less) and the gate-source voltage is very low. However, if an open collector driver is used with a relatively low value of resistance in the collector to improve the switching speed, the "0" state gate-source voltage may be high enough to significantly increase I_{DSS}.

Due to the considerable variations in I_{DSS} as a function of T_J, V_{GS} and V_{TH} from one device to another, it is difficult to quantify this effect in advance of the actual design. The designer will need to look at the actual circuit to see if there is a problem when the device is being operated in a radiation environment or if V_{GS} is substantially greater than zero during the OFF time.

In a radiation environment, $V_{GS(th)}$ is progressively reduced as the dosage is increased. This can dramatically increase I_{DSS}, and it is recommended that I_{DSS} be reduced by applying a negative V_{GS} during the OFF time.

Dissipation Due to Gate Drive

A portion of the gate drive power (P_{Gi}) will be dissipated internally by the device due to the internal gate resistance. The portion of the total gate drive power (P_G) dissipated in the device depends on the internal gate resistance (R_G), and the external drive source resistance (R_S) and may be expressed as:

$$P_{Gi} = P_G\left(\frac{R_G}{R_S + R_G}\right)$$

$$P_{Gi} = V_{GS}\,Q_G\,f_s\left(\frac{R_G}{R_S + R_G}\right) \qquad (6)$$

R_G is typically 1 to 10Ω. For switching rates below 100kHz, P_{Gi} is very small and may be ignored, but as the switching rate is increased, R_S must be reduced to obtain faster transition times, and P_G is increased due to the faster switching rate. In addition, the amount of V_{GS} overdrive is often increased to further reduce the transition times. The net result is that P_{Gi} may be significant especially for switching frequencies above 500kHz.

Conduction Power Loss

The major power loss in a MOSFET is P_C. The conduction loss is:

$$P_C = I^2_{D(RMS)}\,R_{DS(on)} \qquad (7)$$

Equation (7) is deceptively simple. In many applications, I_D will be a duty cycle modulated triangular or trapezoidal waveform, and the designer must calculate the RMS value of the drain current. $R_{DS(on)}$ is a function of I_D, T_J and V_{GS}, and T_J is itself a function of P_T.

The data sheet provides graphs for determining $R_{DS(on)}$. Figure 4 shows $R_{DS(on)}$ as a function of V_{GS} and I_D at T_J = 25°C, and Figure 5 shows the normalized value of $R_{DS(on)}$ as a function of T_J.

The first step is to divide $I_{D(RMS)}$ and V_{GS} and then the value of $R_{DS(on)}$ at 25°C [$R_{DS(on)25°C}$] can be taken from Figure 4. If T_J is known, then the appropriate multiplier for $R_{DS(on)25°C}$ can be found from Figure 5 and P_C calculated directly from equation (7). Note that Figure 5 is for a particular value of I_D and V_{GS}. The curve does not change very much for variations in I_D, but it is strongly affected by changes in V_{GS} when V_{GS} is close to $V_{GS(th)}$. The value of V_{GS} selected for the data sheet curve is well above $V_{GS(th)}$ and as long as the designer uses a value of V_{GS} equal to or greater than the curve value, then little error will occur.

Instead of using Figure 6, an analytical expression for $R_{DS(on)}$ can be used:

$$R_{DS(on)} \cong R_{DS(on)}\,25°\mathrm{C}\left(1+\frac{\alpha}{100}\right)^{T_J-25} \quad (8)$$

The dashed line on Figure 5 is a plot of equation (8) with $\alpha = 0.7$. The fit of the equation is very good above 25° C, but below 25° C the fit becomes quite poor. Figure 5 is for an IRF431 which is a 450V device. Figure 6 shows the normalized $R_{DS(on)}$ curve for an IRF151, a 100V device. Using an α of 0.4, the fit is very good, and the analytic expression for $R_{DS(on)}$ is quite accurate. As the examples in Figure 5 and 6 show, both the shape of the $R_{DS(on)}$ curve and the value for α, vary from one device type to another and for each value of V_{GS}. In order to determine α, it is necessary to have the $R_{DS(on)}$ versus temperature curve, but if one has the curve, then there is no real need for an analytic solution since the graphical solution is simpler and will produce answers of sufficient accuracy. For those who wish an analytic solution using equation (8), Table I is a tabulation of solutions to that equation.

The solution for P_C is not so easy if T_J is not defined. In a typical application, the properties of the heatsink may be defined and the designer must then calculate both P_C and T_J for a variety of load and line conditions. In this case, P_C is in part determined by P_S, P_L and P_G and the solution has to include these losses. Fortunately, there is a simple graphical solution method.

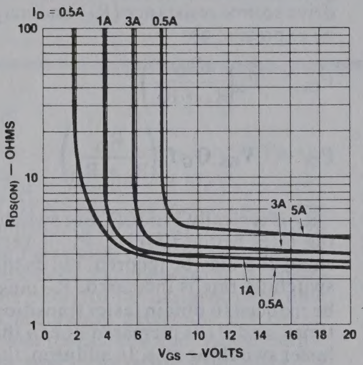


Figure 4. $R_{DS(ON)}$ Dependence on I_D

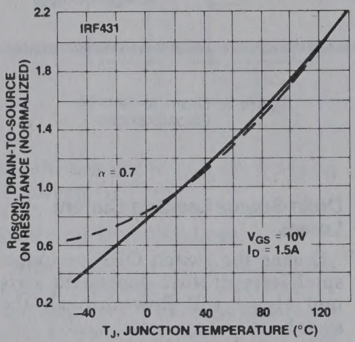


Figure 5. Normalized On-Resistance Vs. Temperature (IRF431)

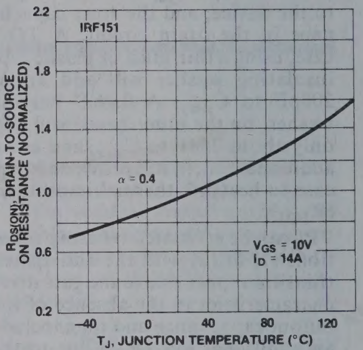


Figure 6. Normalized On-Resistance Vs. Temperature (IRF151)

Table I

		$R_{DS(on)}$ NORMALIZED														
T_J °C T_A = 25° C	ΔT_J °C	α = 0.30	α = 0.35	α = 0.40	α = 0.45	α = 0.50	α = 0.55	α = 0.60	α = 0.65	α = 0.70	α = 0.75	α = 0.80	α = 0.85	α = 0.90	α = 0.95	α = 1.00
-40	-65	0.82	0.80	0.77	0.75	0.72	0.70	0.68	0.66	0.64	0.62	0.60	0.58	0.56	0.54	0.52
-20	-45	0.87	0.85	0.84	0.82	0.80	0.78	0.76	0.75	0.73	0.71	0.70	0.68	0.67	0.65	0.64
0	-25	0.93	0.92	0.91	0.89	0.88	0.87	0.86	0.85	0.84	0.83	0.82	0.81	0.80	0.79	0.78
25	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
40	15	1.05	1.05	1.06	1.07	1.08	1.09	1.09	1.10	1.11	1.12	1.13	1.14	1.14	1.15	1.16
60	35	1.11	1.13	1.15	1.17	1.19	1.21	1.23	1.25	1.28	1.30	1.32	1.34	1.37	1.39	1.42
80	55	1.18	1.21	1.25	1.28	1.32	1.35	1.39	1.43	1.47	1.51	1.55	1.59	1.64	1.68	1.73
100	75	1.25	1.30	1.35	1.40	1.45	1.51	1.57	1.63	1.69	1.75	1.82	1.89	1.96	2.03	2.11
120	95	1.33	1.39	1.46	1.53	1.61	1.68	1.77	1.85	1.94	2.03	2.13	2.23	2.34	2.46	257
140	115	1.41	1.49	1.58	1.68	1.77	1.88	1.99	2.11	2.23	2.36	2.50	2.65	2.80	2.97	3.14
160	135	1.50	1.60	1.71	1.83	1.96	2.10	2.24	2.40	2.56	2.74	2.93	3.14	3.35	3.58	3.83
180	155	1.59	1.72	1.86	2.01	2.17	2.34	2.53	2.73	2.95	3.18	3.44	3.71	4.01	4.33	4.68
200	175	1.69	1.84	2.01	2.19	2.39	2.61	2.85	3.11	3.39	3.70	4.03	4.40	4.80	5.23	5.70

Graphical Solution for MOSFET Thermal Design

From the earlier discussion:

$$P_T = P_S + P_L + P_G + P_C \qquad (9)$$

For convenience, one can lump together the fixed losses*:

$$P_l = P_S + P_L + P_G \qquad (10)$$

Substituting equations (7) and (10) in equation (9):

$$P_T = P_l + I^2_{D(RMS)}\, R_{DS(on)} \qquad (11)$$

From thermal considerations:

$$T_J = T_A + R_{\theta JA}\, P_T \qquad (12)$$

and

$$R_{\theta JA} = R_{\theta HA} + R_{\theta CH} + R_{\theta JC} \qquad (13)$$

**This example ignores the temperature dependent nature of P_L on the assumption that it is negligible or that the worst case value is used.*

To determine P_C and T_J requires the simultaneous solution of equations (11) and (12). This can be done graphically as shown in Figure 7.

If P_l and $I_{D(RMS)}$ are presumed constant over the range of T_J the shape of the P_T versus T_J curve is determined by $R_{DS(on)}$. Except for a scale factor and an offset, the curve for P_T is exactly the same as that shown in Figures 5 and 6.

The scale factor is:

$$K_1 = I^2_{D(RMS)}\, R_{DS(on)\,25^\circ C} \qquad (14)$$

The offset is:

$$K_2 = P_l$$

Then the total power dissipation is:

$$P_T = K_1\, R_{DS(on)normalized} + K_2$$

The curve for equation (2) is simply a straight line with slope of $1/R_{\theta JA}$ and which intersects the T_J axis at $T_J = T_A$.

$$\frac{1}{R_{\theta JA}} = \left(\frac{P_T}{T_J - T_A}\right) \qquad (15)$$

The intersection of the two curves is the desired solution. Figure 7 clearly demonstrates the effect of increasing $R_{\theta JA}$. As $R_{\theta JA}$ is increased, both P_T and T_J increases. A point is reached where there may be two intersections of the curves at T_{J1} and T_{J2}.

T_{J2} represents a point of stable thermal equilibrium and T_{J2} represents an unstable equilibrium point. That this is so can be seen by inspection of Figure 7 as follows:

1. Stable equilibrium can exist only if the heat input (P_T) from the switch equals the heat dissipated by the sink.
2. For $T_J < T'_{J2}$ P_T exceeds the heat removed by the sink. T_J must therefore rise, increasing P_T, until $T_J = T'_{J2}$ where P_T equals the heat removed.
3. For $T'_{J2} < T_J < T'_{J2}$ the heat removed by the sink is greater than P_T and the device must cool down, reducing P_T, until $T_J = T'_{J2}$.
4. If $T_J > T'_{J2}$ then P_T is always greater than the heat removed. P_T and T_J will then increase without limit until the device is destroyed. This is a thermal runaway condition.

As long as the initial temperature is less than T'_{J2} then T_J will converge at T'_{J2}. If $R_{\theta JA}$ is further increased to $R_{\theta JA2}$, there is no intersection of the curves and this also represents a condition of thermal runaway, since P_T is always greater than the heat removed by the heatsink.

Design Example 1

Device = IRF431
$R_{\theta JC}$ = 1.7 deg. C/W
$R_{\theta CH}$ = 0.4 deg. C/W
$R_{\theta HA}$ = 2 deg. C/W and 4 deg. C/W
$I_{D(RMS)}$ = 2.1A
$R_{DS(on)25^\circ C}$ = 1.7Θ (max. $R_{DS(on)}$ at I_D = 3A)
T_A = 55°C
P_l = 0

Find T_J and P_T for each value of $R_{\theta HA}$.

$R_{\theta JA}$ = $R_{\theta JC} + R_{\theta CH} + R_{\theta HA}$
$R_{\theta JA1}$ = 4.1 deg. C/W
$R_{\theta JA2}$ = 6.1 deg. C/W

The graphical solution is shown in Figure 8. For $R_{\theta HA}$ = 2 deg. C/W, P_T = 14.5W and T_J = 115° C. For $R_{\theta HA}$ = 4 deg. C/W, there is no intersection and the device will experience thermal runaway.

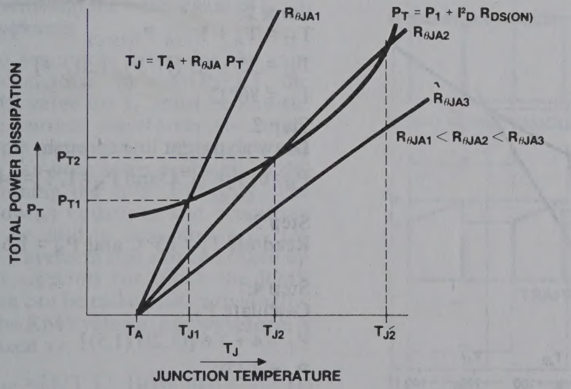


Figure 7. Graphical Representation of the Thermal Equations

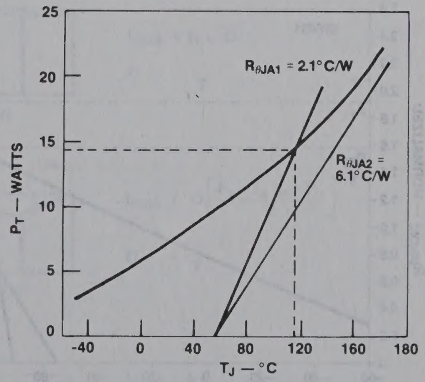


Figure 8. Design Example 1

Suppose one wishes to set P_1 to some value other than zero or to vary I_D. The solution method used in Figure 8 would require the graphs to be redrawn for each new condition. It would be preferable if the normalized ON-resistance versus temperature graph could be used directly without a change of scale for all solutions. The P_T and T_J calculations could then be done directly on the data sheet curves, adding only straight lines. This can be done by normalizing the P_T scale.

At any temperature:

$$P_T = P_1 + I^2_{D(RMS)} R_{DS(on)} \qquad (16)$$

At 25° C:

$$P_{T(25°C)} = P_1 + I^2_{D(RMS)} R_{DS(on)25°C} \qquad (17)$$

Reordering equations (16) and (17):

$$P_T - P_1 = I^2_{D(RMS)} R_{DS(on)} \qquad (18)$$

$$P_{T(25°C)} - P_1 = I^2_{D(RMS)} R_{DS(on)25°C} \qquad (19)$$

Dividing equation (18) by equation (19):

$$\frac{P_T - P_1}{P_{T(25°C)} - P_1} = \frac{R_{DS(on)}}{R_{DS(on)25°C)}} \qquad (20)$$

$= R_{DS(on)N} =$ normalized value of $R_{DS(on)}$ as given in the data sheet graph.

If we then define the normalized power P_N:

$$P_N \cong \frac{P_T - P_1}{P_{T(25°C)} - P_1} = R_{DS(on)N} \qquad (21)$$

$$P_N = R_{DS(on)N}$$

The vertical scale of the $R_{DS(on)}$ normalized scale is now numerically equal to P_N.

In a similar fashion, the second equation can be normalized:

$$T_J = T_A + R_{\theta JA}\, P_T \qquad (23)$$

Rearranging equation (21):

$$P_T = P_1 + P_N\,[P_{T(25°C)} - P_1] \qquad (24)$$

Equation (24) may be simplified to:

$$P_T = P_1 + P_N\,[I^2_{D(RMS)} \cdot R_{DS(on)25°C}] \qquad (25)$$

And then combine equations (23) and (25):

$$T_J = T_A + R_{\theta JA}\,[P_1 + P_N \cdot (I^2_{D(RMS)}\, R_{DS(on)25°C})] \qquad (26)$$

Once a graphical solution in terms of P_N is found, T_J may be read out directly and P_T can be calculated from equation (25).

Design Example 2

Refer to Figure 9.

Device = IRF431
$R_{\theta JC}$ = 1.7 deg. C/W
$R_{\theta CH}$ = 0.4 deg. C/W
$R_{\theta HA}$ = 2 deg. C/W
$R_{DS(on)25°C)}$ = 1.7Ω at 2.1A and 1.5Ω at 1.2A

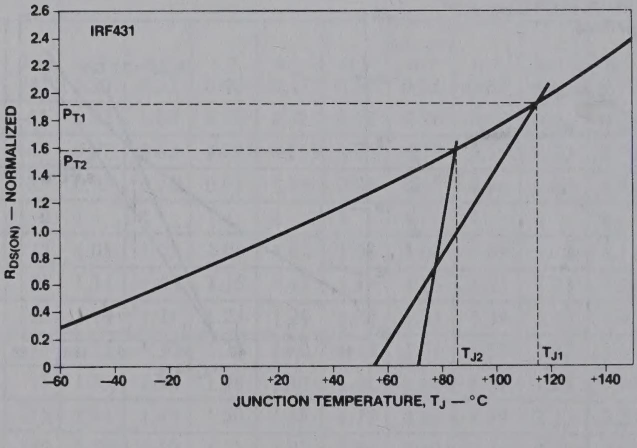


Figure 9. Design Example 2

T_A = 55° C
$I_{D(RMS)}$ = 2.1 and 1.2A
P_1 = 0W and 4W
Find T_J and P_T for each case.

Solution 1

Step 1:
Locate two points on the graph to plot equation (26):

Point 1: For $P_N = 0$, $T_J = T_A$

Point 2: For $P_N = 1$

$$T_J = T_A + R_{\theta JA}\, I^2_{D(RMS)}\, R_{DS(on)25°C}$$

$$T_J = 55° + (4.1)\,(2.1^2)\,(1.7) = 86° C$$

Step 2:
Draw a straight line through:

$P_N = 0$, $T_J = 55°$ C and $P_N = 1$, $T_J = 86°$ C

Step 3:
Read T_J directly off, $T_J = 115°$ C

$P_N = 1.9$

Step 4:
Calculate P_T

$$P_T = P_1 + I^2_{D(RMS)}\, R_{D(on)25°C}\, P_N$$

$$P_T = 0 + (2.2^2)\,(1.7)\,(1.9)$$

$$P_T = 14.5W$$

Solution 2

$I_{D(RMS)}$ is reduced to 1.2A and P_1 is increased to 4W. T_A remains at 55° C.

Step 1:
Find two points for equation (26) with $P_N = 0$ and $P_N = 1$.

Point 1:

$$T_{J1} = T_A + R_{\theta JA}\, P_1$$

$$T_{J1} = 55 + (4.1)\,(4)$$

$$T_{J1} = 71° C$$

Point 2:

$$T_{J2} = T_A + R_{\theta JA}\, P_{T(25°C)}$$

$$T_{J2} = 55 + 4.1\,[(1.2^2)\,(1.5) + 4]$$

$$T_{J2} = 80° C$$

Step 2:
Draw a straight line through:

$P_N = 0$, $T_J = 71°$ C and $P_N = 1$, $T_J = 64°$ C

Step 3:
Read off $T_J = 85°$ C and $P_N = 1.6$

Step 4:
Calculate P_T

$$P_T = 4 + 1.6\,[(1.2^2)\,(1.5)]$$

$$P_T = 7.5W$$

Determination of the Peak Junction Temperature for Pulsed Current Waveforms

The previous discussion and examples were for the average junction temperature. For very long (> 1 sec.), high duty cycle pulses or very short

($< 10\mu s$) pulses, the peak junction temperature is very nearly equal to the average junction temperature, and the procedure is acceptable. For other operating conditions, the procedure is identical, but the equation (26) must be modified to use the transient thermal resistance, $Z_{\theta JC}$. $Z_{\theta JC}$ is related to $R_{\theta JC}$ by:

$$Z_{\theta JC} = r(t)\ R_{\theta JC} \qquad (27)$$

where r(t) is the normalizing factor taken from the normalized transient thermal impedance curves for the particular device. The appropriate values for the pulse width (t_p) and duty cycle (D) must be used.

Equation (26) can now be modified to:

$$T_J = T_A + (r(t)\ R_{\theta JC} + R_{\theta CA})\,[P_1 + P_N\,(I^2_{D(RMS)}\ R_{DS(on)25^\circ C})] \qquad (28)$$

The procedure is exactly as shown earlier except that equation (28) is used instead of equation (26).

Summary

The power loss calculation for a power MOSFET differs substantially from the same calculation for a bipolar power transistor primarily because of the $I^2_{D(RMS)}\ R_{DS(on)}$ loss characteristic. The calculation is further complicated by the non-linear behavior of $R_{DS(on)}$ versus T_J. Because the $R_{DS(on)}$ characteristic must be determined experimentally for each device type, a strictly algebraic approach to the loss calculation is very cumbersome. The graphical method shown here is much more rapid and is just as accurate.

APPENDIX

Determining the RMS Value of I_D Waveforms

To accurately determine the conduction losses in a MOSFET, the RMS value for I_D must be known. The current waveforms are rarely simple sinusoidal or rectangles, and this can pose some problems in determining the value for I_{RMS}. The following equations and procedure can be used to determine I_{RMS} for any waveform that can be broken up into segments for which the RMS value can be calculated individually.

The RMS value of any waveform is defined as:

$$I_{RMS} = [1/T \textstyle\int_0^\tau [I(t)]^2\,dt]^{1/2} \qquad (1)$$

Figure A-1 shows several simple waveforms and the derivation for I_{RMS} using equation (1).

If the actual waveform can be approximated satisfactorily by combining the waveforms in Figure A-1, then the RMS value of the waveform can be calculated from:

$$I_{RMS} = \sqrt{I^2_{RMS(1)} + I^2_{RMS(2)} + \ldots + I^2_{RMS(N)}} \qquad (2)$$

In some applications such as switching regulators, it is possible for the designer to control the wave shape to some extent. This can be very beneficial in reducing the value for I_{RMS} in the switch for a given value of average current (I_{AVG}).

Effect of Waveform Shape on RMS Value

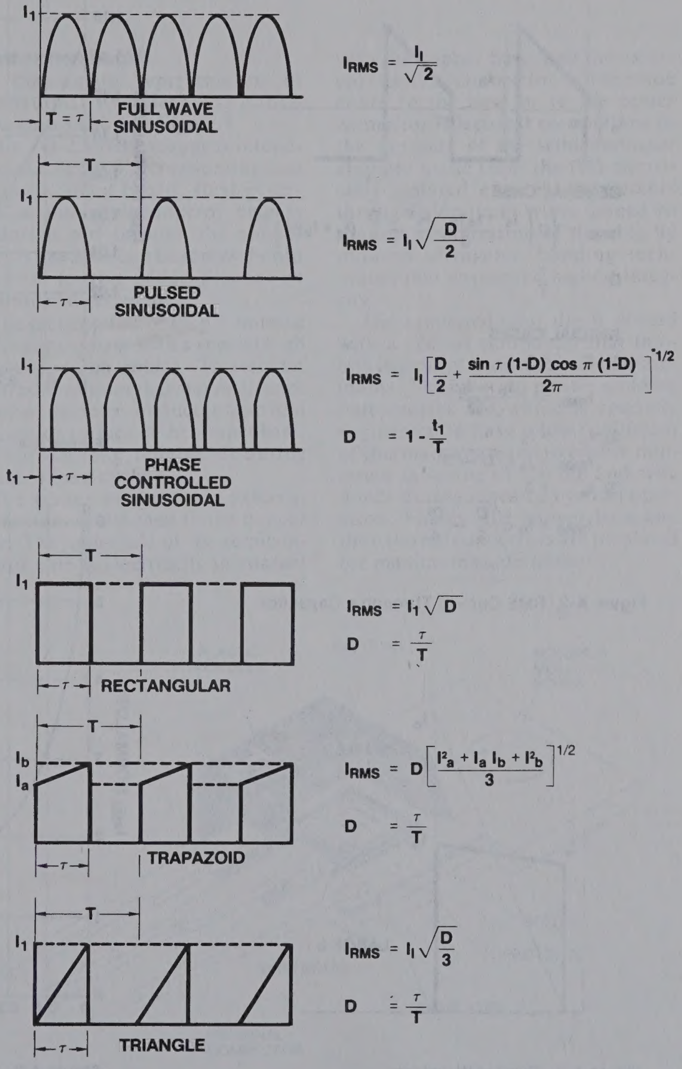
In a switch mode converter, the current waveforms through the inductors, transformer windings, rectifiers and switches will appear as shown in Figure A-2, ranging from a triangle to a rectangle depending on the value of the averaging inductor and the load. For the capacitors, the waveforms will be similar, except that there can be no DC component as shown in Figure A-3. The RMS and average values of the waveform are given in the figures.

It can be shown that:

$$K = \frac{I_a}{I_b} = f\,(L/L_c) \qquad (3)$$

where:

L = inductance of the average choke.



I_1
$I_{RMS} = \frac{I_1}{\sqrt{2}}$
T = τ
FULL WAVE SINUSOIDAL
T
I_1
$I_{RMS} = I_1\sqrt{\frac{D}{2}}$
τ
PULSED SINUSOIDAL
I_1
$I_{RMS} = I_1\left[\frac{D}{2} + \frac{\sin\tau\,(1-D)\cos\pi\,(1-D)}{2\pi}\right]^{1/2}$
$D = 1 - \frac{t_1}{T}$
t_1
τ
PHASE CONTROLLED SINUSOIDAL
T
I_1
$I_{RMS} = I_1\sqrt{D}$
$D = \frac{\tau}{T}$
τ
RECTANGULAR
T
I_b
I_a
$I_{RMS} = D\left[\frac{I^2_a + I_a I_b + I^2_b}{3}\right]^{1/2}$
$D = \frac{\tau}{T}$
τ
TRAPAZOID
T
I_1
$I_{RMS} = I_1\sqrt{\frac{D}{3}}$
$D = \frac{\tau}{T}$
τ
TRIANGLE

Figure A-1.

$L_c = 1$ is the critical inductance for a particular input voltage and load power.

As L is increased, K goes from 0 (triangle) to 1 (rectangle). Substituting $K = I_a/I_b$, for the continuous choke current case:

$$I_{RMS} = \frac{2\ I_{(avg)}}{\sqrt{D}} \sqrt{\frac{K^2 + K + 1}{3\ (K + 1)^2}} \qquad (4)$$

For constant $I_{(avg)}$ and D, the normalized ($I_{RMS} = 1$ for $K = 1$) I_{RMS} is as shown in Figure A-4. This curve shows that, for triangular current waveforms, the I^2R losses are 32% higher than for rectangular waveforms. It is also apparent that for $I_a/I_b > 0.6$, the additional losses incurred by having $L < \alpha$ is only 2%, so from a practical point of view, L need only be about twice L_c. Increasing the value of I_a/I_b increases the switch turn-on losses but decreases the turn-off losses. Since the turn-off losses frequently dominate, increasing I_a/I_b reduces the total switch loss also.

For the case of discontinuous inductor current ($L < L_c$), $I_a/I_b = 0$ and is no longer relevant, since the waveforms are now triangles. For a given $I_{(avg)}$ the RMS current is:

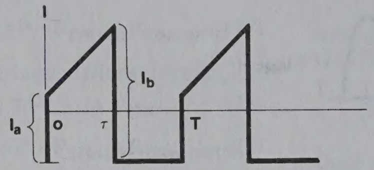
$$I_{RMS} = \frac{2\ I_{(avg)}}{\sqrt{3D}}$$

A plot of equation (4) is given in Figure A-5, where $I_{(avg)}$ is constant and I_{RMS} is normalized to $D = 1$. Obviously, triangular current waveforms with high peak currents and low duty cycles are to be avoided if low losses are desired.

For the case where: $I_a = I_b$:

$$I_{RMS} = \frac{I_{(avg)}}{\sqrt{3D}}$$

the curve in Figure A-5 also applies. It is important to realize that for a given input voltage, current and transformation ratio, there can be a difference in duty cycle which allows one circuit to have lower losses due to the lower value of I_{RMS}.



GENERAL CASE

$$I_{RMS} = \left\{ D \left[\frac{I_a^2 + I_a I_b + I_b^2}{3} - \frac{D}{4} (I_a + I_b)^2 \right] \right\}^{1/2}$$

$$D = \frac{\tau}{T}$$

SPECIAL CASES

1) $D = 1$

$$I_{RMS} = \frac{I_b - I_a}{\sqrt{12}}$$

2) $I_a = I_b$

$$I_{RMS} = I_a \sqrt{D - D^2}$$

3) $I_a = 0$

$$I_{RMS} = I_b \sqrt{\frac{D}{3} - \frac{D^2}{4}}$$

Figure A-2. RMS Current Through a Capacitor

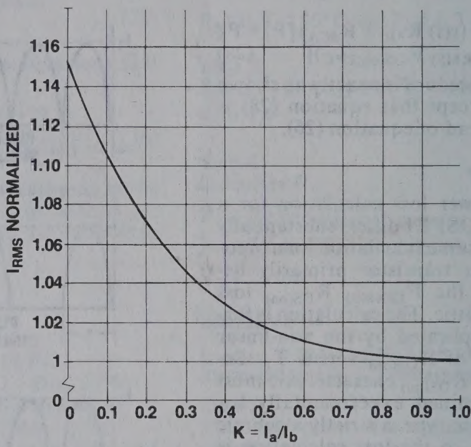


Figure A-4. Variation of I_{RMS} with Squareness Ratio

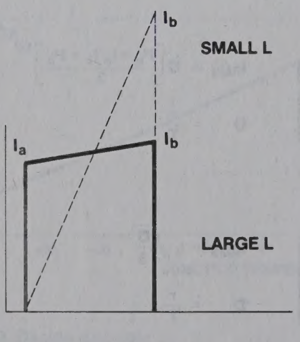


Figure A-3. Current Waveform

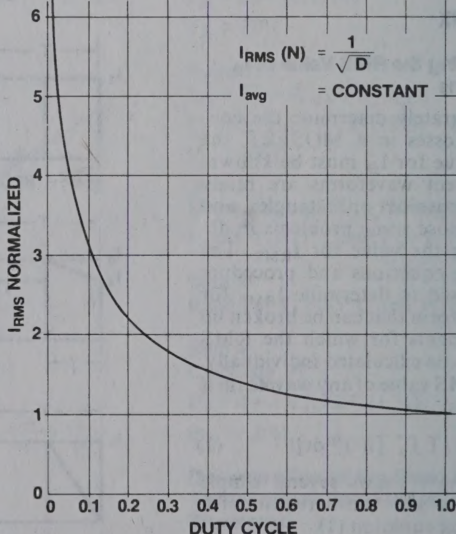


Figure A-5. Variation of I_{RMS} Valve with Duty Cycle

CHAPTER 10
APPLICATION NOTE 932

Reliability . . . the key to IR's TO-220 devices

Introduction

International Rectifier has available a wide variety of semiconductor devices in the compact, economical TO-220AB package. These include a full range of HEXFET™s, high voltage fast switching bipolar transistors, and Schottky rectifiers. This application note is concerned primarily with the TO-220AB plastic package itself, and specifically the question of *reliability* — a subject which is of paramount importance to semiconductor users.

Unlike metal packages, a plastic package is not intrinsically hermetic. This could potentially invite ingress of moisture and contaminants, and possible degradation of the semiconductor.

Because of this potential hazard, it is essential that manufacturers pay special attention to the design, construction, and quality control of these products. Provided they do so, the performance and reliability can be equally as good as that of other types of packages.

IR engineers have carefully designed IR's TO-220AB plastic package to take full advantage of the most modern assembly techniques, materials, and design concepts. The viability of IR's TO-220AB products has been convincingly demonstrated by an arduous program of reliability and endurance tests. IR is confident that the performance of these products meets or exceeds all accepted industry standards.

This application note describes the basic design features of IR's TO-220AB package, discusses how it is assembled, and outlines the quality control procedures employed. Also described are various reliability and endurance tests to which IR subjects these parts, with typical test results given.

Construction Details

A diagramatic representation of International Rectifier's TO-220AB package is shown in Figure 1.

The TO-220AB package is intended primarily for direct mounting into a printed circuit board. Heat generated in the semiconductor chip is conducted out through the copper base. A heatsink can be screwed onto this base to give added dissipation capability, if required.

The semiconductor chip is bonded to the copper base with a special high tensile strength solder. This solder ensures minimum thermal resistance between the semiconductor chip and the outside surface of the copper base, and ensures long, reliable life during repeated load cycling.

The center of the three external connectors is attached to the copper base. The underside of the semiconductor chip is electrically in contact with the copper base, and the external electrical connection can be made either to the base or to the center connector. Electrical connections to the top side of the semiconductor chip are made from the two electrically isolated external connectors through aluminum wires, joined to the top metallization of the chip by modern ultrasonic bonding techniques that ensure the highest integrity.

The semiconductor die is coated with a special compound that inhibits ingress of moisture and contaminants. The external plastic molding that encases the whole is specially engineered to have a low coefficient of thermal expansion to ensure minimum fatiguing of the die and wire bonds during repeated cyclical operation. Finally, the copper base and the external connectors are tin plated for maximum solderability.

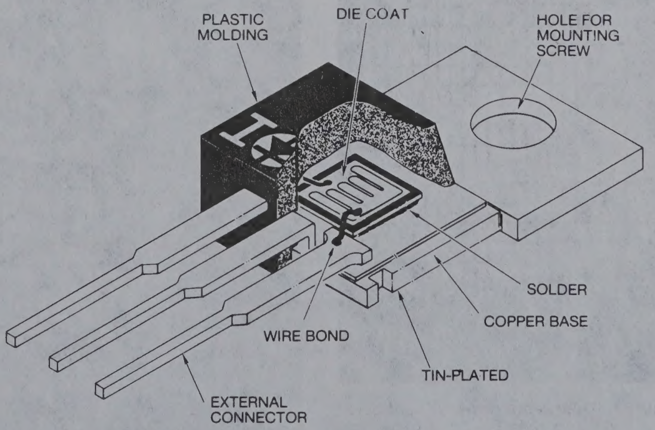


Figure 1. TO-220AB cutaway view of an IR power transistor.

In-Line Quality Control

IR's basic philosophy is that quality must be *designed into* a product; it cannot be "tested in" at the end of the production line. Hand in hand with this basic approach to quality, IR maintains a rigid in-line inspection program. A brief description of the main process steps, and the corresponding in-line quality control procedures, follows (refer to the simplified assembly flow chart shown in Figure 2).

Each discrete semiconductor chip is obtained from a much larger wafer of silicon, which typically may contain several hundred chips. A photograph of a typical wafer is shown in Figure 3. All wafers are probed at an automatic station to a given set of electrical specifications. Figure 4 shows a photograph of an automatic wafer probe station. During electrical probing, the dice are inked for identification, and then scribed for separation.

After scribing, the chips are visually inspected, and then passed to the header assembly and chip bonding ("solder-down") stages. A sample is then taken to assure die bonding integrity.

The next step is ultrasonic bonding of the aluminum wires that make the electrical connections to the top of the chip. In-process quality assurance (QA) at wire bond operation incorporates destructive and non-destructive wire pull as well as visual inspection of the wire bond at the chip and the leads.

The chips are then covered with a "die coat" compound, and cured. A further QA inspection is then performed. This is followed by molding the plastic package, deflashing, post-mold cure, and a further QA inspection. The external connections are then *tin plated* and *trimmed*, and QA inspection is again carried out.

Final electrical tests are then carried out, to specified limits. A computer-controlled tester automatically checks the devices and sorts them into different categories according to the programmed specification. Included is a power test to ensure the specified thermal resistance limit of the device. Controls are continually maintained to assure the integrity of the tester and its programming. After final test the parts are marked with the International Rectifier logo and the part number of the device. A final sample QA test is then performed for specified electrical parameters. In addition to electrical inspection, mechanical and visual inspection is carried out on every lot.

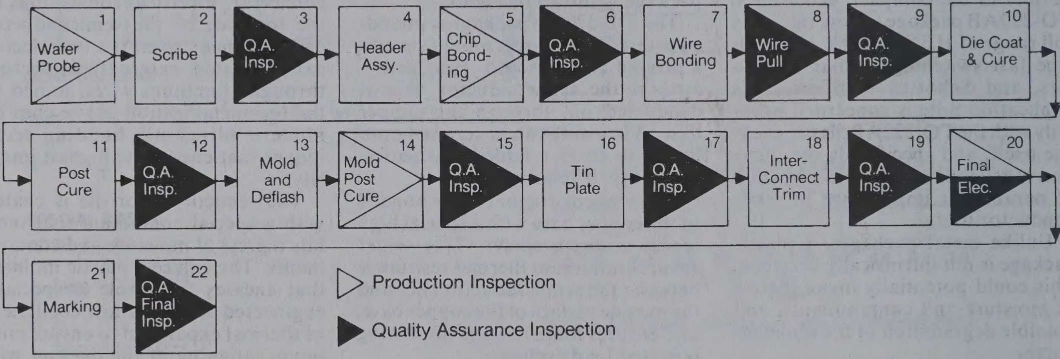


Figure 2. Simplified process flow chart shows in-line QC inspection steps during TO-220 assembly and testing.

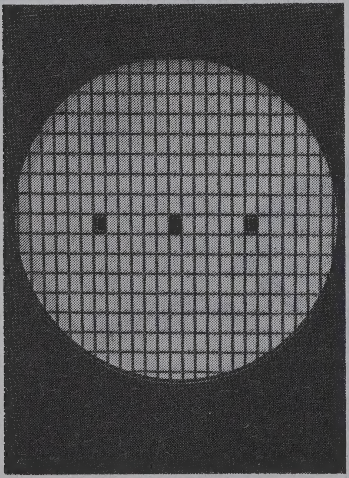


Figure 3. This photo shows the configuration of the HEX-2 dice pattern on a 3-inch diameter HEXFET silicon wafer.

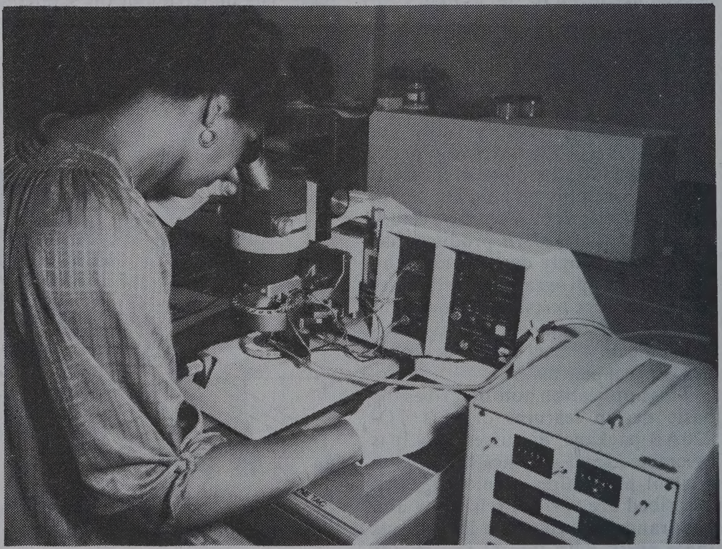


Figure 4. One of the automatic wafer probe stations used to perform electrical testing with the aid of a computer-controlled Teradyne tester.

Reliability Tests

International Rectifier TO-220 products are subjected to a series of arduous reliability tests to check and recheck their integrity. These tests are designed to simulate much more extreme operating conditions than would actually be encountered in most practical applications. Satisfactory performance under these stringent tests ensures completely reliable, trouble-free operation in any practical equipment.

The following describes the reliability tests that are routinely applied to these devices, and typical test results that are obtained.

High Temperature Reverse Bias (HTRB)

The HTRB test is designed to check the stability of the device under "reverse bias" conditions of the main blocking junction at high temperature, as a function of time.

The junction surface stability of a device is dependent upon the passivation of the blocking junction. This includes the preparation and cleaning of the junction surface prior to passivation, the properties of the passivating material, and the coating that is applied over the whole chip for protection of non-passivated areas.

The stability of leakage current over a period of time, for a given temperature and voltage applied across the junction, is indicative of junction surface stability. It is therefore a good indicator of device quality and reliability.

For bipolar transistors, voltage is applied across the collector to base junction, with the emitter open. I_{CBO} is the important parameter to monitor, rather than I_{CEO}. This is because I_{CEO} is dependent upon gain which increases with temperature. When testing power HEXFETs, voltage is applied between drain and source, and I_{DSS} is monitored. The gate is shorted to the source, to prevent damage due to buildup of charges on the gate.

The leakage current of a stable device should remain relatively constant, or increase slightly over the period of the test, which is typically of 1000 hours duration.

The final high temperature leakage current must be less than a given specified maximum value. A failure occurs when the leakage increases beyond this level. A catastrophic failure occurs when the leakage reaches such a high level that the power dissipation causes the device to go into thermal runaway and destroy itself.

Figure 5 shows a typical HTRB test equipment console. Typical results of HTRB tests on specific batches of IR's TO-220AB package devices are shown in Table 1.

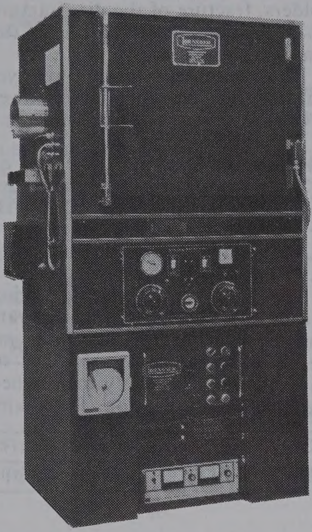


Figure 5. High Temperature Reverse Bias (HTRB) tester designed to check the junction stability of power semiconductor devices.

Power Cycling

The purpose of this test is to determine the integrity of the chip/package assembly to repeated heating and cooling under power — as is normally experienced when the equipment in which the device is installed is cycled on and off, or when the dissipation in the device is varied over a long period compared to the time constant of the package and/or attached heatsink.

DC power is applied to the device until the desired junction temperature is reached. The power is then switched off, and forced air cooling applied until the junction temperature decreases to ambient temperature. The sequence is repeated until the specified number of cycles is performed. The temperature excursion is carefully maintained for repeatability of results.

The power cycling test identifies the degree of thermal fatigue of the solder bond interfaces between the chip and the mounting surface, between the chip and the wire connection, and between the wire and the external connector.

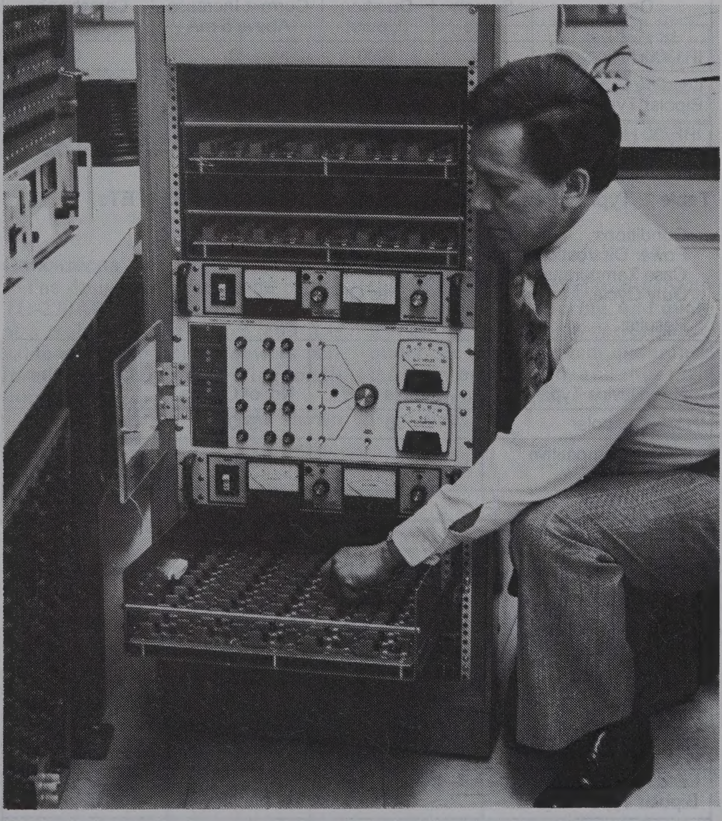


Figure 6. Power Cycling equipment used to test the integrity of the chip/package assembly.

For bipolar transistors, test parameters that are monitored to determine performance are thermal resistance, base-emitter voltage, forward bias safe operating area, collector-emitter saturation voltage, and collector-to-base leakage current. These are measured and recorded at the start of the test, and then at regular intervals.

For power HEXFETs, parameters used to monitor performance are thermal resistance, threshold voltage, on-resistance, gate-to-source leakage current, and drain-to-source leakage current. Those used for rectifiers are thermal resistance, forward voltage drop, and leakage current.

A catastrophic failure occurs when thermal fatigue causes the thermal resistance or the conduction voltage to increase beyond the maximum value specified on the data sheet. Thermal fatigue failure usually results in fracture and crystallization of solders, fracture of the die, fracture of the wire bond, or shorting of the main blocking junciton.

Figure 6 shows typical power cycling test gear. Typical results of power cycling tests are shown in Table 2.

Temperature Cycling

The purpose of this test is to determine the resistance of TO-220AB devices to high and low temperature exposures and the effects of alternate exposures to these extremes.

The test is performed by placing the devices alternately in separate chambers set for high and low temperatures. The air temperature of each chamber is evenly maintained by means of circulation. The chambers have sufficient thermal capacity so that the specified ambient is reached within two minutes after the devices have been transferred to the chamber.

The number of cycles is determined by the severity of the expected environment. It is commonly accepted in the industry that ten cycles is sufficient to determine the quality of the device.

Each cycle consists of an exposure to one extreme temperature for 15 minutes minimum, then 5 minutes maximum at 25° C between chambers, then 15 minutes minimum at the other extreme, then back again to room temperature for a maximum of 5 minutes.

Temperature cycling identifies any excessive strains set up between materials; it does not test the fatigue resistance, as does power cycling. Effects of thermal cycling on weak TO-220AB devices include cracking of the silicon die, changes in electrical characteristics due to mechanical displacements, ruptured leads and metallization, and degradation of passivation.

Electrical parameters that are checked to monitor performance are generally the same as for the power cycling test. In addition, the bonding of the wires to the chip are checked at the conclusion of the test.

A catastrophic failure occurs when there is a change in the device's parameters beyond specified levels, or when the TO-220AB device checks electrically as "open", caused by cracking of the die or other mechanical damage.

Typical results of temperature cycling tests are shown in Table 3.

Thermal Shock

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature.

The parts, in a mesh basket, are alternately immersed in baths of liquid, maintained at 0° C and 100° C. They are kept for five minutes in each bath, and a maximum of ten seconds is allowed for transfer between the baths.

This test produces sudden heating in the TO-220AB device, and produces unusual stresses due to the short-term temperature gradients that are set up. Generally, a total of five cycles is sufficient to determine quality of the device.

Effects of thermal shock include die cracking, changes in electrical characteristics due to mechanical displacement, metallization problems, ruptured leads, and degradation of passivation.

Table 1: Typical HTRB Results on Bipolars and HEXFETs

Conditions:
Junction Temperature = 150° C
Applied Voltage = 300V

Results:

Device Type	Sample Size	Test Duration (Hours)	No. of Devices Showing Leakage Current Increase Above 5 mA	Number of Catastrophic Failures
IR13006 Bipolar	25	1000	0	0
Leading Compet. Bipolar Type	25	1000	19	1
IRF730 HEXFET	50	1000	0	1

Table 2: Typical Power Cycling Results on Bipolars and HEXFETs

Conditions:
Power Dissipation: 2.5W
Case Temperature Excursion: 80° C
Duty Cycle: 1 minute ON, 2.5 minutes OFF

Results:

Device Type	Sample Size	No. of Cycles	Number of Catastrophic Failures
IR13006 Bipolar	50	5000	1
Leading Competitive Bipolar Type	50	5000	3
IRF730 HEXFET	50	5000	0

Table 3: Typical Temperature Cycling Results on Bipolars and HEXFETs

Conditions:
150° C: 15 minutes, 25° C: 15 minutes, -55° C: 15 minutes, 25° C: 5 minutes

Results:

Device Type	Sample Size	No. of Cycles	Number of Catastrophic Failures
IR13006 Bipolar	50	10	0
Leading Competitive Bipolar Type	20	10	1
IRF730 HEXFET	45	10	0

Parameters that are checked to monitor performance are the same as for the temperature cycling test, and a catastrophic failure is determined in the same way.

Typical results of thermal shock tests are shown in Table 4.

"Pressure Cooker" Test

The purpose of the "pressure cooker" test is to determine the resistance of the component to moisture by subjecting it to relatively high steam pressure levels.

A standard domestic pressure cooker, providing a pressure of 15 lbs/sq. in. over atmospheric, can be used. A wire mesh tray is constructed inside to keep the TO-220AB devices about two inches above the surface of deionized water and to prevent condensed water from collecting on them.

After reaching working value, the pressure is maintained for four hours. The devices are then removed, blown dry, and washed in methanol to remove surface moisture before data is recorded.

This test is becoming an industry standard because of the ease with which it can be performed and because of its ability to produce rapid results.

Parameters that are usually monitored are leakage current, thermal resistance, and voltage drop.

Typical results of this test are summarized in Table 5.

Salt Spray Test

The purpose of this test is to determine the resistance of the part to ingress of salt solution, and to corrosion on exposed and interior surfaces.

The parts are suspended for 24 hours in a mist of 20% salt solution such that liquid cannot collect on them. Parameters that are typically monitored to check performance are leakage current and "saturation" or "conduction" voltage.

Table 6 shows typical results.

Table 4: Typical Thermal Shock Results on Bipolars and HEXFETs

Conditions:
100° C: 5 minutes, 0° C: 5 minutes

Results:

Device Type	Sample Size	No. of Cycles	Number of Catastrophic Failures
IR13006 Bipolar	10	5	0
Leading Competitive Bipolar Type	10	5	0
IRF730 HEXFET	10	5	0

Table 5: Typical "Pressure Cooker" Results on Bipolars and HEXFETs

Conditions:
Pressure: 15 lbs/in.^{2}

Results:

Device Type	Sample Size	Test Duration	Number of Catastrophic Failures
IR13006 Bipolar	40	4 hours	0
IRF730 HEXFET	40	4 hours	0

Table 6: Typical Salt Spray Results on Bipolars and HEXFETs

Conditions:
MIL-STD 750 Method 1041
Mist 20% Salt Solution

Results:

Device Type	Sample Size	Test Duration	Number of Catastrophic Failure
IR13006 Bipolar	10	24 hours	0
IRF730 HEXFET	10	24 hours	0

Conclusions

The design features of the plastic TO-220AB package differ from those of a truly hermetic device, and it is valid to ask how these devices perform under arduous operating conditions.

This application note has shown that by proper attention to all aspects of design, manufacturing, and quality control, satisfactory performance under the most stringent endurance tests can be achieved, and thus high reliability in practical, everyday usage is assured. ☐

This application note was co-authored by the following technical staff members of International Rectifier's Application Engineering Department: Brian R. Pelly, Bill Mickelopoulos and Brian Smith.

CHAPTER 11

APPLICATION NOTE 931

Custom Assembly of HEXFET™ Dice

Introduction

This application note describes the HEXFET™ transistors available from International Rectifier in die form. These power MOS field effect transistor dice feature the same high reliability planar technology used for the IRF series of TO-3 and TO-220 packaged HEXFETs. The same advanced MOS processing techniques, silicon gate structure, and efficient hexagonal source pattern are available in die form for hybrid assembly. As the name implies, the HEXFET consists of an hexagonal cell structure which results in a packing density of over 500,000 cells per square inch. Use of a silicon-gate design and state-of-the-art MOS processing techniques result in an extremely reliable device which is highly reproducible in various die sizes. Hybrid packaging of such die results in substantial savings in weight and volume compared to standard packaging.

Die Characteristics

Three HEXFET die sizes presently available from International Rectifier are described in Figure 1. These are termed HEX-2 (90 x 138 mil), HEX-3 (114 x 180 mil), and HEX-5 (250 x 250 mil). Each die size is available in six voltage types with corresponding on-resistances. All die sizes have one gate and one source bonding pad as shown. Each HEXFET die is individually probed at room ambient temperature to the electrical specifications shown in Figure 2.

Because of limitations when electrically probing in wafer form, some of the generic specifications of the equivalent packaged device cannot be tested and guaranteed in die form. These are power dissipation, P_D, safe operating area, SOA, thermal resistance, R_{thJC}, on-resistance at rated current, $R_{DS(on)}$, and inductive current, I_{LM}. (On-resistance at $I_D=1A$ is tested and guaranteed according to Figure 2.) These parameters are dependent upon the user's assembly technique. However, the following characteristics are guaranteed by design to meet the specifications of the equivalent part: g_{fs}, C_{iss}, C_{oss}, C_{rss}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f, and $T_{J(max)}$. Consult the appropriate data sheet from Figure 2.

Following electrical probing, the dice are inked for identification and scribed. The dice are mechanically separated, 100% visually inspected, and packed for shipment.

Handling and Shipping

HEXFET dice from International Rectifier are shipped in anti-static chip trays and sealed in plastic containers for protection during shipment. Once opened, the dice must be stored in a dry, inert atmosphere such as nitrogen prior to assembly. Dice should be handled with DuPont Teflon-tipped vacuum pencils to prevent mechanical damage. Any nonconformance to the electrical or visual inspection specifications in this brochure must be reported in writing to International Rectifier within 60 days after shipment of the lot by International Rectifier. International Rectifier assumes no responsibilities for die which have been subjected to further processing such as mountdown, wire bonding, or encapsulation. In the interest of product improvement, the right is reserved to make design or processing changes without notification.

The anti-static chip trays are designed to avoid the build-up of static charge. International Rectifier HEXFETs have large gate capacitances and thick oxide layers relative to low level MOS devices. Though

HEXFET DIE DIMENSIONS		HEX-2	HEX-3	HEX-5
L_1	mm	3.51	4.57	6.35
	inch	0.138	0.180	0.250
W_1	mm	2.29	2.90	6.35
	inch	0.090	0.114	0.250
L_2	mm	0.51	0.51	1.02
	inch	0.020	0.020	0.040
W_2	mm	0.66	0.69	1.57
	inch	0.026	0.027	0.062
Die Thickness T	mm	0.41	0.41	0.41
	inch	0.016	0.016	0.016
Number of Gate Fingers		4	4	8

L_1, W_1: Dimension Tolerance ±0.2mm ±0.008 in.

$L_2 W_2 T$: Dimension Tolerance ±0.05mm ±0.002 in.

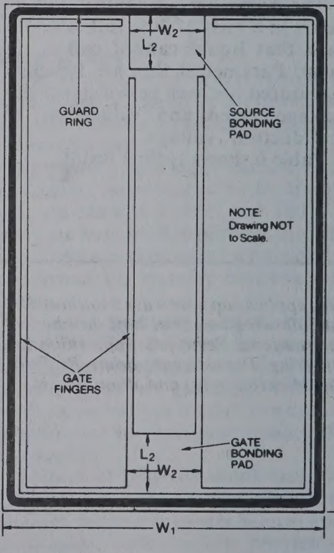


Figure 1. HEXFET Die Dimension Summary and Bonding\Pad Diagram.

significantly more rugged than such low level devices, reasonable precautions should be observed during handling and assembly to prevent exceeding the ± 20V maximum gate-source voltage. The chip tray capacities are 100, 35, and 16 die per tray for HEX-2, HEX-3, and HEX-5 dice, respectively.

Visual Inspection of Die

International Rectifier HEXFET die are designed to meet the visual inspection criteria of Mil-Standard 750B, Method 2072 with the exception of the specific criteria listed below. HEXFET dice are visually screened to a 2.5% AQL level. Mil-Standard 750B, Method 2072 shall apply except as follows (the paragraph numbers refer to Method 2072):

PAR. 3.1 All inspection is at 30X magnification.

PAR. 3.1.1.3 Localized areas of discoloration are generally harmless films which are present in varying degrees from lot to lot and are not cause for rejection.

PAR. 3.1.3.d A die having attached portions of the adjacent die up to 10% of additional length is acceptable, provided the die still fits the chip tray cavity.

PAR. 3.2.3.1 Ink, chemical stains, and other foreign material attached to the surface of the HEXFET die are isolated by a vapox (silicon dioxide) layer, except for the aluminum bonding pads, and are not cause for rejection.

Die Mounting

The HEXFET dice have chromium-nickel-silver drain metallization which is suitable for solder preform mounting using solders such as 95/5 PbSn or 92.5/2.5/5 PbAgIn solder. Any of the commonly used header or substrate materials such as copper, nickel plated copper, and gold plated molybdenum, beryllia, and alumina are acceptable. The substrate must be freed of oxides prior to assembly either by chemical cleaning or H_2 pre-firing techniques. The HEXFET dice should be cleaned prior to mountdown in deionized water cascade (one minute) followed by isopropyl alcohol agitated bath (twice, one minute each) and then 70°C nitrogen chamber drying. Mounting is generally accomplished in a profiled belt furnace. The furnace zone settings will depend upon hybrid mass density, jigging, and belt speed. The HEXFET die temperature must not exceed 400°C, nor be in the range of 350 to 400°C for greater than one minute. A clean furnace of hydrogen atmosphere is recommended, although nitrogen atmosphere or forming gas (nitrogen - hydrogen, 85% - 15%) is acceptable.

Wire Bonding

Electrical connection to the gate and source aluminum bonding pads is by ultrasonic wirebonding with annealed 99% Al, 1% Si wire having an elongation of 10%. The maximum recommended wire diameter for HEX-2, HEX-3, and HEX-5 is 8 mil, 10 mil, and 20 mil, respectively. Caution must be exercised during wire bonding to insure that the bonding footprint remains within the bonding pad area; otherwise, device failure can result. Likewise, wire bond equipment settings should be optimized and a wire pull test performed (e.g., see Method 2037, Mil-Standard 750B) to monitor wire bond strength uniformity. Destructive sample testing and 100% nondestructive testing is recommended. Rebonding of wire bond rejects can be performed although decreased yield can be expected from such reworks. Using process controls as described above, final assembly yields of 80% to 95% can be achieved.

Encapsulation

Prior to encapsulation, the die/assembly must be kept in a moisture-free environment, as I_{GSS} particularly is sensitive to surface moisture. If the final package is non-hermetic, a high grade electronic coating such as Dow Corning RTV3140 or equivalent should be applied. If the package is hermetic, the coating is optional. Cleaning of the die in a freon vapor degreaser prior to coating is recommended. Immediately prior to encapsulation, a 150°C, two hour bake should be performed to remove any surface moisture. Capping of hermetic packages should be performed in a dry, nitrogen atmosphere.

Conclusion

The use of power MOSFET dice for hybrid assemblies can result in significant reduction in overall package size. In addition, the high gain characteristics of the HEXFET can allow further miniaturization by eliminating complex drive circuitry. Several HEXFET dice can readily be mounted on the same heatsink to form circuit configurations or to parallel devices. The HEXFET operational advantages, thereby, can be realized in very compact, custom package configurations.

HEXFET DIE SIZE	PART NUMBER	MAXIMUM RATED V_{DS}	$R_{DS}(on)$ @ $I_D = 1A$ $V_{GS} = 10V$		I_{DSS} @ RATED V_{DS} MAXIMUM	I_{GSS} @ $V_{GS} = 20V$ MAXIMUM	$V_{GS}(TH)$ @ $I_D = 1mA$, $V_{DS} = V_{GS}$		DATA SHEET FOR CORRESPONDING PACKAGED DEVICE
			TYP.	MAX.			MIN.	MAX.	
HEX-2	IRFC123 IRFC122	60V 100V	0.25 Ω	0.4 Ω	1.0mA	100nA	1.5V	3.5V	PD-9.312
	IRFC223 IRFC222	150V 200V	0.5 Ω	1.2 Ω	1.0mA	100nA	1.5V	3.5V	PD-9.316
	IRFC323 IRFC322	350V 400V	1.5 Ω	2.5 Ω	1.0mA	100nA	1.5V	3.5V	PD-9.314
HEX-3	IRFC133 IRFC132	60V 100V	0.14 Ω	0.25Ω	1.0mA	100nA	1.5V	3.5V	PD-9.303
	IRFC233 IRFC232	150V 200V	0.25 Ω	0.6 Ω	1.0mA	100nA	1.5V	3.5V	PD-9.306
	IRFC333 IRFC332	350V 400V	0.8 Ω	1.5 Ω	1.0mA	100nA	1.5V	3.5V	PD-9.302
HEX-5	IRFC153 IRFC152	60V 100V	0.045Ω	0.08Ω	1.0mA	100nA	1.5V	3.5V	PD-9.305
	IRFC253 IRFC252	150V 200V	*	*	1.0mA	100nA	1.5V	3.5V	*
	IRFC353 IRFC352	350V 400V	0.25 Ω	0.4 Ω	1.0mA	100nA	1.5V	3.5V	PD-9.304

Electrical testing AQL level is 2.5%.

**Data available April 1980.*

Figure 2. Electrical Probe Specifications for N-Channel HEXFET Transistor Die.

IOR

INTERNATIONAL RECTIFIER

HEXFET PRODUCT DATA

THE HEXFET DEVICES LISTED IN THIS DATABOOK
REPRESENT THE INTERNATIONAL RECTIFIER POWER MOSFET LINE
AS OF APRIL 1, 1981.

IF YOU WISH TO RECEIVE DATA ON ALL NEW DEVICE AND PACKAGE TYPES
AS ISSUED, COMPLETE AND MAIL THE HEXFET DATA REGISTRATION FORM
WHICH APPEARS AS THE LAST PAGE OF THIS DATABOOK.

HEXFET SELECTOR GUIDE BY VOLTAGE RANGE AND SERIES

TO-3 Package

Voltage Range	Series Number	"On" Resistance	Page Number
60V-100V	IRF120 IRF9130* IRF130 IRF150	0.3Ω 0.3Ω 0.18Ω 0.055Ω	107 199 111 115
150V-200V	IRF220 IRF230 IRF250	0.8Ω 0.4Ω 0.085Ω	119 123 127
350V-400V	IRF320 IRF330 IRF350	1.8Ω 1.0Ω 0.3Ω	131 135 139
450V-500V	IRF420 IRF430 IRF450	3.0Ω 1.5Ω 0.4Ω	143 147 151

Hermetically sealed HEXFETs are available in the industry standard TO-3 (TO-204AA) package for highest thermal conductivity and greatest environmental protection. The 150-watt devices feature an all copper base and heavy 0.063-inch diameter pins.

TO-220 Package

Voltage Range	Series Number	"On" Resistance	Page Number
60V-100V	IRF510 IRF9520* IRF520 IRF9530* IRF530	0.6Ω 0.6Ω 0.3Ω 0.3Ω 0.18Ω	115 203 159 207 163
150V-200V	IRF610 IRF620 IRF630	1.6Ω 0.8Ω 0.4Ω	167 171 175
350V-400V	IRF710 IRF720 IRF730	3.6Ω 1.8Ω 1.0Ω	179 183 187
450V-500V	IRF820 IRF830	3.0Ω 1.5Ω	191 195

The smaller HEXFET dice sizes are available in the TO-220AB case. These devices are ideal for printed circuit board mounting and offer minimum size at minimum cost. Application Note AN-932 describes the reliability features of International Rectifier's advanced TO-220 package design.

*P-Channel

NOTE: The Series Selector shows only the first part number within a series. Refer to appropriate listings for the complete HEXFET line.

TO-3 PACKAGED HEXFETs LISTED BY VOLTAGE RATINGS

N-Channel Types Electrical Characteristics at 25°C

V_{DS} Drain Source Voltage (Volts)	R_{DS}(ON) On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) @ 90% Case	I_{DM} Pulsed Drain Current (Amps)	gfs S Typical Transconductance (Siemens)	C_{iss} Typical Input Capacitance (pf)	P_D Max. Power Dissipation (Watts)	Page
500	0.4	IRF450	10.0	25.0	10.0	2000	150	151
500	0.5	IRF452	8.0	20.0	10.0	2000	150	151
500	1.5	IRF430	3.5	7.0	2.5	700	75	147
500	2.0	IRF432	3.0	6.0	2.5	700	75	147
500	3.0	IRF420	2.0	5.0	1.75	300	40	143
500	4.0	IRF422	1.5	4.0	1.75	300	40	143
450	0.4	IRF451	10.0	25.0	10.0	2000	150	151
450	0.5	IRF453	8.0	20.0	10.0	2000	150	151
450	1.5	IRF431	3.5	6.0	2.5	700	75	147
450	2.0	IRF433	3.0	25.0	2.5	700	75	147
450	3.0	IRF421	2.0	5.0	1.75	300	40	143
450	4.0	IRF423	1.5	4.0	1.75	300	40	143
400	0.3	IRF350	11.0	25.0	9.0	3000	150	139
400	0.4	IRF352	10.0	20.0	9.0	3000	150	139
400	1.0	IRF330	4.0	8.0	3.5	750	75	135
400	1.5	IRF332	3.5	7.0	3.5	750	75	135
400	1.8	IRF320	3.0	6.0	2.0	450	40	131
400	2.5	IRF322	.25	5.0	2.0	450	40	131
350	0.3	IRF351	11.0	25.0	9.0	3000	150	139
350	0.4	IRF353	10.0	20.0	9.0	3000	150	139
350	1.0	IRF331	4.0	8.0	3.5	750	75	135
350	1.5	IRF333	3.5	7.0	3.5	750	75	135
350	1.8	IRF321	3.0	6.0	2.0	450	40	131
350	2.5	IRF323	2.5	5.0	2.0	450	450	131
200	0.085	IRF250	20.0	60.0	12.0	1800	150	127
200	0.120	IRF252	17.0	50.0	12.0	1800	150	127
200	0.4	IRF230	7.0	15.0	4.5	750	75	123
200	0.6	IRF232	6.0	12.0	4.5	750	75	123
200	0.8	IRF220	4.0	10.0	2.3	450	40	119
200	1.2	IRF222	3.5	8.0	2.3	450	40	119
150	0.085	IRF251	20.0	60.0	12.0	1800	150	127
150	0.120	IRF253	17.0	50.0	12.0	1800	150	127
150	0.4	IRF231	7.0	15.0	4.5	750	75	123
150	0.6	IRF233	6.0	12.0	4.5	750	75	123
150	0.8	IRF221	4.0	10.0	2.3	450	40	119
150	1.2	IRF223	3.5	8.0	2.3	450	40	119
100	0.055	IRF150	28.0	70.0	10.0	3000	150	115
100	0.08	IRF152	24.0	60.0	10.0	3000	150	115
100	0.18	IRF130	12.0	30.0	5.0	750	75	111
100	0.25	IRF132	10.0	25.0	5.0	750	75	111
100	0.3	IRF120	6.0	15.0	2.5	450	40	107
100	0.4	IRF122	5.0	12.0	2.5	450	40	107
60	0.055	IRF151	28.0	70.0	10.0	3000	150	115
60	0.8	IRF153	24.0	60.0	10.0	3000	150	115
60	0.18	IRF131	12.0	30.0	5.0	750	75	111
60	0.25	IRF133	10.0	25.0	5.0	750	75	111
60	0.3	IRF121	6.0	15.0	2.5	450	40	107
60	0.4	IRF123	5.0	12.0	2.5	450	40	107

P-Channel Types Electrical Characteristics at 25°C

-100	0.3	IRF9130	-8.0	-30.0	3.5	500	75	199
-100	0.4	IRF9132	-7.0	-25.0	3.5	500	75	199
-60	0.3	IRF9131	-8.0	-30.0	3.5	500	75	199
-60	0.4	IRF9133	-7.0	-25.0	3.5	500	75	199

TO-220AB PACKAGED HEXFETs LISTED BY VOLTAGE RATINGS

N-Channel Types Electrical Characteristics at 25°C

V_{DS} Drain Source Voltage (Volts)	R_{DS}(ON) On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) @ 90% Case	I_{DM} Pulsed Drain Current (Amps)	gfs S Typical Transconductance (Siemens)	C_{iss} Typical Input Capacitance (pf)	P_D Max. Power Dissipation (Watts)	Page
500	1.5	IRF830	3.0	7.0	2.5	700	75	195
500	2.0	IRF832	2.5	6.0	2.5	700	75	195
500	3.0	IRF820	1.5	5.0	1.75	300	40	191
500	4.0	IRF822	1.0	4.0	1.75	300	40	191
450	1.5	IRF831	3.0	7.0	2.5	700	75	195
450	2.0	IRF833	2.5	6.0	2.5	700	75	195
450	3.0	IRF821	1.5	5.0	1.75	300	40	191
450	4.0	IRF823	1.0	4.0	1.75	300	40	191
400	1.0	IRF730	3.5	8.0	3.5	700	75	187
400	1.5	IRF732	3.0	7.0	3.5	700	75	187
400	1.8	IRF720	2.5	6.0	2.0	450	40	183
400	2.5	IRF722	2.0	5.0	2.0	450	40	183
400	3.6	IRF710	1.2	2.4	1.0	135	20	179
400	5.0	IRF712	0.9	2.0	1.0	135	20	179
350	1.0	IRF731	3.5	8.0	3.5	700	75	187
350	1.5	IRF733	3.0	7.0	3.5	700	75	187
350	1.8	IRF721	2.5	6.0	2.0	450	40	183
350	2.5	IRF723	2.0	5.0	2.0	450	40	183
350	3.6	IRF711	1.2	2.4	1.0	135	20	179
350	5.0	IRF713	0.9	2.0	1.0	135	20	179
200	0.4	IRF630	6.0	15.0	4.5	750	75	175
200	0.6	IRF632	5.0	12.0	4.5	750	75	175
200	0.8	IRF620	3.5	10.0	2.3	450	40	171
200	1.2	IRF622	3.0	8.0	2.3	450	40	171
200	1.5	IRF610	2.0	5.0	1.2	135	20	167
200	2.4	IRF612	1.5	4.0	1.2	135	20	167
150	0.4	IRF631	6.0	15.0	4.5	750	75	175
150	0.6	IRF633	5.0	12.0	4.5	750	75	175
150	0.8	IRF621	3.5	10.0	2.3	450	40	171
150	1.2	IRF623	3.0	8.0	2.3	450	40	171
150	1.5	IRF611	2.0	5.0	1.2	135	20	167
150	2.4	IRF613	1.5	4.0	1.2	135	20	167
100	0.18	IRF530	10.0	30.0	5.0	700	75	163
100	0.25	IRF532	8.0	25.0	5.0	700	75	163
100	0.3	IRF520	5.0	15.0	2.5	450	40	159
100	0.4	IRF522	4.0	12.0	2.5	450	40	159
100	0.6	IRF510	3.0	8.0	1.5	135	20	155
100	0.8	IRF512	2.5	6.0	1.5	135	20	155
60	0.18	IRF531	10.0	30.0	5.0	700	75	163
60	0.25	IRF533	8.0	25.0	5.0	700	75	163
60	0.3	IRF521	5.0	15.0	2.5	450	40	159
60	0.4	IRF523	4.0	12.0	2.5	450	40	159
60	0.6	IRF511	3.0	8.0	1.5	135	20	155
60	0.8	IRF513	2.5	6.0	1.5	135	20	155

P-Channel Types Electrical Characteristics at 25°C

-100	0.3	IRF9530	-7.0	-30.0	3.5	500	75	207
-100	0.4	IRF9532	-6.0	-25.0	3.5	500	75	207
-100	0.6	IRF9520	-4.0	-15.0	1.8	300	40	203
-100	0.8	IRF9522	-3.5	-12.0	1.8	300	40	203
-60	0.3	IRF9531	-7.0	-30.0	3.5	500	75	207
-60	0.4	IRF9533	-6.0	-25.0	3.5	500	75	207
-60	0.6	IRF9521	-4.0	-15.0	1.8	300	40	203
-60	0.8	IRF9523	-3.5	-12.0	1.8	300	40	203

TO-3 PACKAGED HEXFETs LISTED IN NUMERICAL ORDER

N-Channel Types Electrical Characteristics at 25°C

Part Numbers	V_{DS} Drain Source Voltage (Volts)	R_{DS}(ON) On-State Resistance (Ohms)	I_D Continuous Drain Current (Amps) @ 90°C Case	I_{DM} Pulsed Drain Current (Amps)	P_D Max. Power Dissipation (Watts)	gfs Typical Transconductance S (Amps/Volt)	C_{iss} Typical Input Capacitance (pf)	Page
IRF120	100	0.3	6.0	15.0	40	2.5	450	107
IRF121	60	0.3	6.0	15.0	40	2.5	450	107
IRF122	100	0.4	5.0	12.0	40	2.5	450	107
IRF123	60	0.4	5.0	12.0	40	2.5	450	107
IRF130	100	0.18	12.0	30.0	75	5.0	750	111
IRF131	60	0.18	12.0	30.0	75	5.0	750	111
IRF132	100	0.25	10.0	25.0	75	5.0	750	111
IRF133	60	0.25	10.0	25.0	75	5.0	750	111
IRF150	100	0.055	28.0	70.0	150	10.0	3000	115
IRF151	60	0.055	28.0	70.0	150	10.0	3000	115
IRF152	100	0.08	24.0	60.0	150	10.0	3000	115
IRF153	60	0.08	24.0	60.0	150	10.0	300	115
IRF220	200	0.8	4.0	10.0	40	2.3	450	119
IRF221	150	0.8	4.0	10.0	40	2.3	450	119
IRF222	200	1.2	3.5	8.0	40	2.3	450	119
IRF223	150	1.2	3.5	8.0	40	2.3	450	119
IRF230	200	0.4	7.0	15.0	75	4.5	750	123
IRF231	150	0.4	7.0	15.0	75	4.5	750	123
IRF232	200	0.6	6.0	12.0	75	4.5	750	123
IRF233	150	0.6	6.0	12.0	75	4.5	750	123
IRF250	200	0.085	20.0	60.0	150	12.0	1800	127
IRF251	150	0.085	20.0	60.0	150	12.0	1800	127
IRF252	200	0.120	17.0	50.0	150	12.0	1800	127
IRF253	150	0.120	17.0	50.0	150	12.0	1800	127
IRF320	400	1.8	3.0	6.0	40	2.0	450	131
IRF321	350	1.8	3.0	6.0	40	2.0	450	131
IRF322	400	2.5	2.5	5.0	40	2.0	450	131
IRF323	350	2.5	2.5	5.0	40	2.0	450	131
IRF330	400	1.0	4.0	8.0	75	3.5	750	135
IRF331	350	1.0	4.0	8.0	75	3.5	750	135
IRF332	400	1.5	3.5	7.0	75	3.5	750	135
IRF333	350	1.5	3.5	7.0	75	3.5	750	135
IRF350	400	0.3	11.0	25.0	150	9.0	3000	139
IRF351	350	0.3	11.0	25.0	150	9.0	3000	139
IRF352	400	0.4	10.0	20.0	150	9.0	3000	139
IRF353	350	0.4	10.0	20.0	150	9.0	3000	139
IRF420	500	3.0	2.0	5.0	40	1.75	300	143
IRF421	450	3.0	2.0	5.0	40	1.75	300	143
IRF422	500	4.0	1.5	4.0	40	1.75	300	143
IRF423	450	4.0	1.5	4.0	40	1.75	300	143
IRF430	500	1.5	3.5	7.0	75	2.5	700	147
IRF431	450	1.5	3.5	7.0	75	2.5	700	147
IRF432	500	2.0	3.0	6.0	75	2.5	700	147
IRF433	450	2.0	3.0	6.0	75	2.5	700	147
IRF450	500	0.4	10.0	25.0	150	10.0	2000	151
IRF451	450	0.4	10.0	25.0	150	10.0	2000	151
IRF452	500	0.5	8.0	20.0	150	10.0	2000	151
IRF453	450	0.5	8.0	20.0	150	10.0	2000	151

P-Channel Types Electrical Characteristics at 25°C

IRF9310	-100	0.3	-8.0	-30.0	75	3.5	500	199
IRF9131	-60	0.3	-8.0	-30.0	75	3.5	500	199
IRF9132	-100	0.4	-7.0	-25.0	75	3.5	500	199
IRF9133	-60	0.4	-7.0	-25.0	75	3.5	500	199

NOTE: The IRF9130 Family is an Electrical Complement to the IRF120 Family.

TO-220 PACKAGED HEXFETs LISTED IN NUMERICAL ORDER

N-Channel Types Electrical Characteristics at 25°C

Part Numbers	V_{DS} Drain Source Voltage (Volts)	R_{DS}(ON) On-State Resistance (Ohms)	I_D Continuous Drain Current (Amps) @ 90°C Case	I_{DM} Pulsed Drain Current (Amps)	P_D Max. Power Dissipation (Watts)	gfs Typical Transconductance S (Amps/Volt)	C_{iss} Typical Input Capacitance (pf)	Page
IRF510	100	0.6	3.0	8.0	20	1.5	135	155
IRF511	60	0.8	3.0	8.0	20	1.5	135	155
IRF512	100	0.8	2.5	6.0	20	1.5	135	155
IRF513	60	0.8	2.5	6.0	20	1.5	135	155
IRF520	100	0.3	5.0	15.0	40	2.5	450	159
IRF521	60	0.3	5.0	15.0	40	2.5	450	159
IRF522	100	0.4	4.0	12.0	40	2.5	450	159
IRF523	60	0.4	4.0	12.0	40	2.5	450	159
IRF530	100	0.18	10.0	30.0	75	5.0	700	163
IRF531	60	0.18	10.0	30.0	75	5.0	700	163
IRF532	100	0.25	8.0	25.0	75	5.0	700	163
IRF533	60	0.25	8.0	25.0	75	5.0	700	163
IRF610	200	1.5	2.0	5.0	20	1.2	135	167
IRF611	150	1.5	2.0	5.0	20	1.2	135	167
IRF612	200	2.4	1.5	4.0	20	1.2	135	167
IRF613	150	2.4	1.5	4.0	20	1.2	135	167
IRF620	200	0.8	3.5	10.0	40	2.3	450	171
IRF621	150	0.8	3.5	10.0	40	2.3	450	171
IRF622	200	1.2	3.0	8.0	40	2.3	450	171
IRF623	150	1.2	3.0	8.0	40	2.3	450	171
IRF630	200	0.4	6.0	15.0	75	4.5	750	175
IRF631	150	0.4	6.0	15.0	75	4.5	750	175
IRF632	200	0.6	5.0	12.0	75	4.5	750	175
IRF633	150	0.6	5.0	12.0	75	4.5	750	175
IRF710	400	3.6	1.2	2.4	20	1.0	135	179
IRF711	350	3.6	1.2	2.4	20	1.0	135	179
IRF712	400	5.0	0.9	2.0	20	1.0	135	179
IRF713	350	5.0	0.9	2.0	20	1.0	135	179
IRF720	400	1.8	2.5	6.0	40	2.0	450	183
IRF721	350	1.8	2.5	7.0	40	2.0	450	183
IRF722	400	2.5	2.0	5.0	40	2.0	450	183
IRF723	350	2.5	2.0	5.0	40	2.0	450	183
IRF730	400	1.0	3.5	8.0	75	3.5	700	187
IRF731	350	1.0	3.5	8.0	75	3.5	700	187
IRF732	400	1.5	3.0	7.0	75	3.5	700	187
IRF733	350	1.5	3.0	7.0	75	3.5	700	187
IRF820	500	3.0	1.5	5.0	40	1.75	300	191
IRF821	450	3.0	1.5	5.0	40	1.75	300	191
IRF822	500	4.0	1.0	4.0	40	1.75	300	191
IRF823	450	4.0	1.0	4.0	40	1.75	300	191
IRF830	500	1.5	3.0	7.0	75	2.5	700	195
IRF831	450	1.5	3.0	7.0	75	2.5	700	195
IRF832	500	2.0	2.5	6.0	75	2.5	700	195
IRF833	450	2.0	2.5	6.0	75	2.5	700	195

P-Channel Types Electrical Characteristics at 25°C

IRF9520	-100	0.6	-4.0	-15.0	40	1.8	300	203
IRF9521	60	0.6	-4.0	-15.0	40	1.8	300	203
IRF9522	-100	0.8	-3.5	-12.0	40	1.8	300	203
IRF9523	-60	0.8	-3.5	-12.0	40	1.8	300	203
IRF9530	-100	0.3	-7.0	-30.0	75	3.5	500	207
IRF9531	-60	0.3	-7.0	-30.0	75	3.5	500	207
IRF9532	-100	0.4	-6.0	-25.0	75	3.5	500	207
IRF9533	-60	0.4	-6.0	-25.0	75	3.5	500	207

NOTE: The IRF9530 Family is an Electrical Complement to the IRF520 Family.

The Current Ratings of HEXFETs as compared to Bipolar Transistors and other available power MOSFETs.

The criteria upon which International Rectifier bases the continuous current I_D ratings of HEXFETs are quite different to those traditionally used for bipolar transistors. Whereas the continuous collector current rating of a bipolar transistor does not normally represent a practically useable level of operating current, the I_D rating for IR's HEXFETs shown on the data sheets in this book are practically USEABLE ratings.

Limiting Factors in Bipolar Transistor Current Ratings.

The published collector current rating of a bipolar transistor cannot normally be fully utilized because the gain is typically quite low at rated current at normal operating junction temperature, while the switching losses and saturation voltage drop are inconveniently high. In fact, the rated continuous collector current of a bipolar transistor is based upon specified values of saturation voltage drop and gain at a junction temperature of 25°C — a quite unrealisitc temperature for normal operation. Peak design operating current for a bipolar is typically 60% — 70% of the published continuous rating.

HEXFETs can be Operated to Full Rated Currents.

HEXFETs are not limited either by gain or by switching energy. The major criterion on which the continuous current rating of a HEXFET is based is purely thermal. The current that is permitted to flow through a HEXFET is limited only to the extent that the junction temperature must not exceed the rated $T_{J\,max}$ (150°C). The lower the case temperature — that is, the better the cooling — the greater is the permitted case to junction temperature rise, the greater is the allowed internal power dissipation, and the greater is the permissable current. Rated current I_D at any give case temperature T_C for a HEXFET is given by:

$$I_D = \sqrt{\frac{T_{J\,max}\;T_C}{R_{DS\,(on)}\;R_{thJC}}}$$

Where $R_{DS\,(on)}$ is the maximum value of the on-resistance at rated $T_{J\,(max)}$ and R_{thJC} is the maximum value of the internal junction to case thermal resistance. As an example, Figure 1 shows the relationship between current rating I_D and case temperature T_C for the IRF330 HEXFET. Note that below a case temperature of 25°C, the I_D rating is limited by the current carrying capacity of the internal bonding wires.

Rating for Realistic Operating Temperatures.

When International Rectifier introduced power HEXFETs it was decided that their published continuous I_D current ratings should reflect genuine useable levels which could be achieved with typical practical heat sinks. We therefore chose to assign nominal I_D current ratings to all HEXFETs which corresponded to a nominal case temperature of 90°C. The I_D ratings which appear on all the HEXFET data sheets in this book reflect this nominal case temperature, and as such are REAL RATINGS which can be FULLY UTILIZED in most practical applications.

Bipolar derating factors do not apply.

Unfortunately, designers familiar with the "derating" factors normally necessary for bipolar transistors often do not appreciate that the published I_D ratings of IR's HEXFETs are USEABLE RATINGS. Sometimes this leads to the choice of a HEXFET which is larger and more costly than really needed, simply because the designer applies the same derating factors to which he has become accustomed with bipolar transistors.

Ratings at 25°C Case are unrealistic.

Unfortunately, too, other power MOSFET manufacturers generally have not adopted the same conservative ground rules used by IR for their published I_D ratings. Typically, competitive current ratings are based upon the unrealistically low case temperature of 25°C, while the internal dissipation heats the junction to $T_{J\,max.}$ (usually 150°C). The heatsink required to implement this set of conditions would be impractical; such continuous I_D ratings serve only as benchmarks, and do not represent practically useable ratings.

Because of these competitive practices, misunderstandings can arise when comparing HEXFETs with other power MOSFETs. In order to provide a benchmark for comparison of HEXFETs with other manufacturer's power MOSFETs, Table 1 shows current ratings for IR's HEXFETs for a case temperature of 25°C, alongside the "useable" ($T_C \cong 90$°C) data sheet I_D ratings.

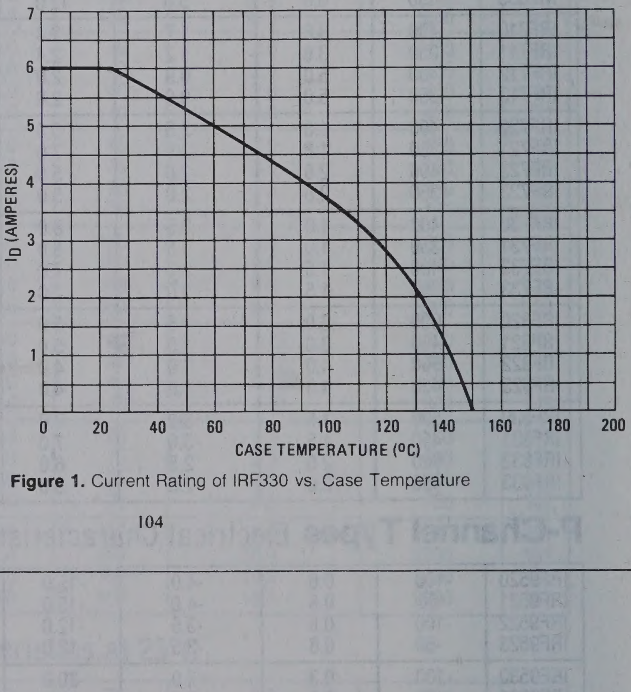


Figure 1. Current Rating of IRF330 vs. Case Temperature

Table 1. HEXFET Current Ratings at 25°C and 90°C Case Temperatures

HEXFET DEVICE TYPE	$R_{DS(on)}$ @T_J = 25°C OHMS	NORM $R_{DS(on)}$ Factor @T_J = 150°C	$R_{DS(on)}$ @T_J = 150°C OHMS	θJC °C/W	I_D RATING On Data Sheet @ 90°C Case Amps	I_D RATING @ 25°C Case Amps
IRF510,511	0.6	2.0	1.2	6.4	3.0	4.0
IRF512,513	0.8	2.0	1.6	6.4	2.5	3.5
IRF610,611	1.5	2.1	3.15	6.4	2.0	2.5
IRF612,613	2.4	2.1	5.04	6.4	1.5	2.0
IRF710,711	3.6	2.3	8.28	6.4	1.2	1.6
IRF712,713	5.0	2.3	11.5	6.4	0.9	1.3
IRF120,121/520,521	0.3	2.0	0.6	3.12	6.0/5.0	8.0
IRF122,123/522,523	0.4	2.0	0.8	3.12	5.0/4.0	7.0
IRF220,221/620,621	0.8	2.1	1.68	3.12	4.0/3.5	5.0
IRF222,223/622,623	1.2	2.1	2.52	3.12	3.5/3.0	4.0
IRF320,321/720,721	1.8	2.3	4.14	3.12	3.0/2.5	3.0
IRF322,323/722,723	2.5	2.3	5.75	3.12	2.5/2.0	2.5
IRF420,421/820,821	3.0	2.5	7.5	3.12	2.0/1.5	2.5
IRF422,423/822,823	4.0	2.5	10.0	3.12	1.5/1.0	2.0
IRF130,131/530,531	0.18	2.0	0.36	1.67	12/10	14
IRF132,133/532,533	0.25	2.0	0.5	1.67	10/8	12
IRF230,231/630,631	0.4	2.1	0.84	1.67	7/6	9
IRF232,233/632,633	0.6	2.1	1.26	1.67	6/5	8
IRF330,331/730,731	1.0	2.2	2.2	1.67	4/3.5	6
IRF332,333/732,733	1.5	2.2	3.3	1.67	3.5/3	5
IRF430,431/830,831	1.5	2.3	3.45	1.67	3.5/3	5
IRF432,433/832,833	2.0	2.3	4.6	1.67	3/2.5	4
IRF150,151	0.055	1.7	0.0935	0.83	28	40
IRF152,153	0.08	1.7	0.136	0.83	24	33
IRF250,251	0.085	2.0	0.17	0.83	20	30
IRF252,253	0.12	2.0	0.24	0.83	17	25
IRF350,351	0.3	2.2	0.66	0.83	11	15
IRF352,353	0.4	2.2	0.88	0.83	10	13
IRF450,451	0.4	2.2	0.88	0.83	10	13
IRF452,453	0.5	2.2	1.1	0.83	8	12
IRF9520,9521	0.6	1.85	1.11	3.12	-4.0	-6.0
IRF9522,9523	0.8	1.85	1.48	3.12	-3.5	-5.0
IRF9130,9131/9530,9531	0.3	1.85	0.555	1.67	-8.0	-12
IRF9132,9133/9532,9533	0.4	1.85	0.74	1.67	-7.0	-10

HEXFET DEVICE CHARACTERISTICS AND RATINGS.

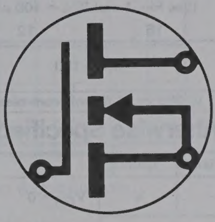
The HEXFET devices listed in this DATABOOK represent the International Rectifier power MOSFET line as of April 1, 1981. Some changes to earlier published Data Sheets have been made. Therefore the data presented here supersedes all previous specifications.

Reference is made to all previous Data Sheets in the upper corner of each page beginning a specific series. This will permit holders of previous materials to compare the current data with that appearing on the earlier Data Sheets, if necessary.

In the interest of product improvement, International Rectifier reserves the right to change specifications at any time without notice.

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF120 IRF121 IRF122 IRF123



N Channel

100 Volt, 0.30 Ohm HEXFET™

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

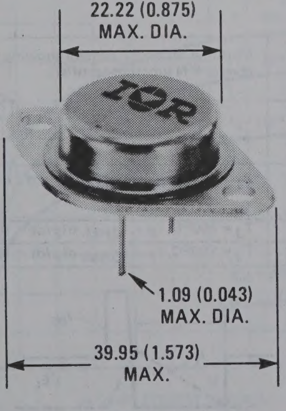
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

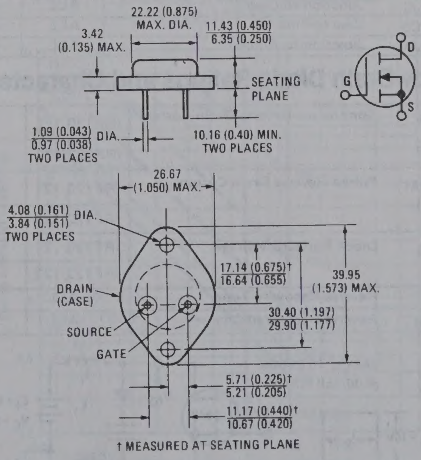
Product Summary

Part Number	V_{DS}	R_{D} (on)	I_D
IRF120	100V	0.30Ω	6A
IRF121	60V	0.30Ω	6A
IRF122	100V	0.40Ω	5A
IRF123	60V	0.40Ω	5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings

	Parameter	IRF120	IRF121	IRF122	IRF123	Units
V_{DS}	Drain — Source Voltage	100	60	100	60	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	100	60	100	60	V
I_D @ $T_C \cong 89.5°C$	Continuous Drain Current	6	6	5	5	A
I_{DM}	Pulsed Drain Current	15	15	12	12	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	40 (See Fig. 11)				W
	Linear Derating Factor	0.32 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH				A
		15	15	12	12	
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10 s)				°C

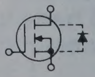
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF120 IRF122	100	—	—	V	$V_{GS} = 0$
		IRF121 IRF123	60	—	—	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	0.1	1.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0$
			—	0.2	4.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, T_J = 125°C
$I_{D\ (on)}$	On-State Drain Current	IRF120 IRF121	8.0	—	—	A	V_{DS} = 25V, V_{GS} = 10V
		IRF122 IRF123	7.0	—	—	A	
$R_{DS\ (on)}$	Static Drain-Source On State Resistance	IRF120 IRF121	—	0.25	0.30	Ω	V_{GS} = 10V, I_D = 3A
		IRF122 IRF123	—	0.30	0.40	Ω	
g_{fs}	Forward Transconductance	ALL	1.5	2.5	—	S (℧)	V_{DS} = 25V, I_D = 3A
C_{iss}	Input Capacitance	ALL	—	450	600	pF	$V_{GS} = 0$, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	50	100	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	—	20	40	ns	I_D = 3A, E_1 = 0.5 BV_{DSS}
t_r	Rise Time	ALL	—	35	70	ns	(See Fig. 13)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	T_J = 125°C (MOSFET switching times are essentially
t_f	Fall Time	ALL	—	35	70	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	0.2	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF120, 121	—	—	6.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF122, 123	—	—	5.0		
I_{DRM}	Pulsed Reverse Drain Current	IRF120, 121	—	—	15	A	
		IRF122, 123	—	—	12		
V_{SD}	Diode Forward Voltage	IRF120, 121	—	—	1.90	V	T_J = 25°C, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF122, 123	—	—	1.70		
t_{rr}	Reverse Recovery Time	ALL	—	150	—	ns	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.0	—	μC	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

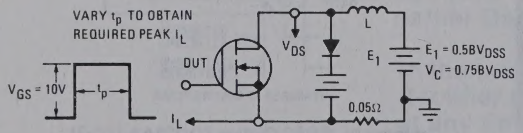


Fig. 1 — Clamped Inductive Test Circuit

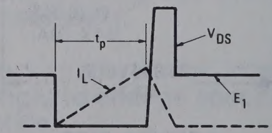


Fig. 2 — Clamped Inductive Waveforms

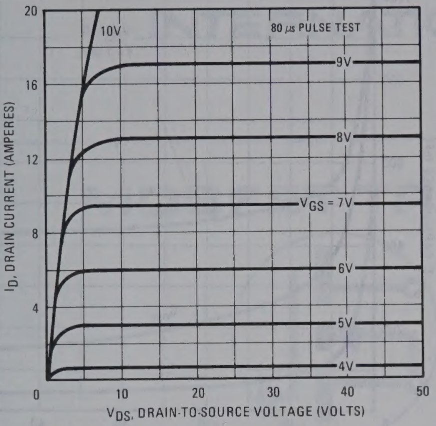


Fig. 3 — Typical Output Characteristics

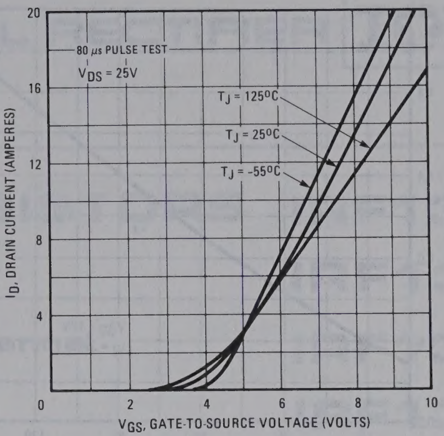


Fig. 4 — Typical Transfer Characteristics

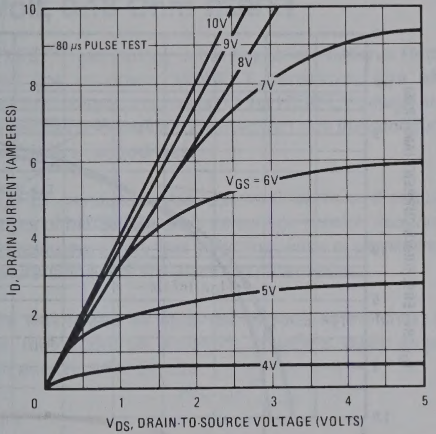


Fig. 5 — Typical Saturation Characteristics
(IRF120, IRF121)

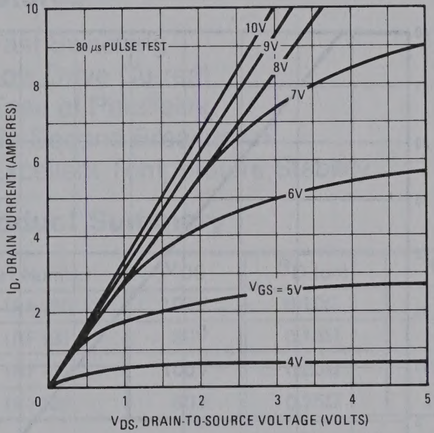


Fig. 6 — Typical Saturation Characteristics
(IRF122, IRF123)

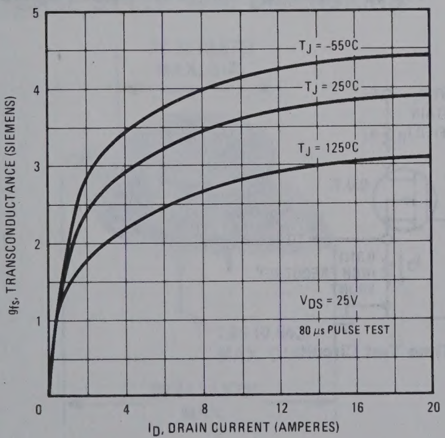


Fig 7. — Typical Transconductance Vs. Drain Current

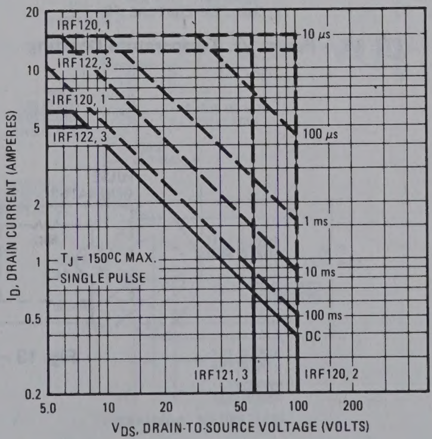


Fig. 8 — Maximum Safe Operating Area

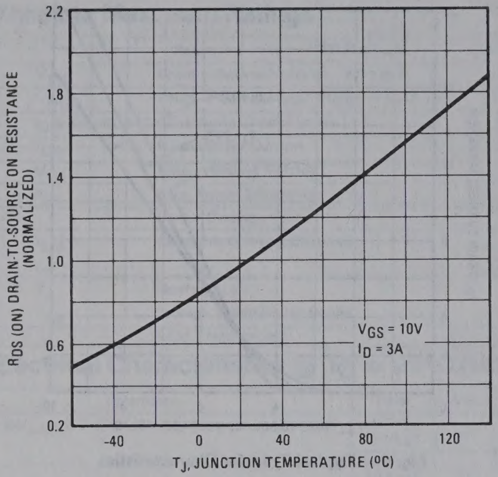


Fig. 9 — Normalized On-Resistance Vs. Temperature

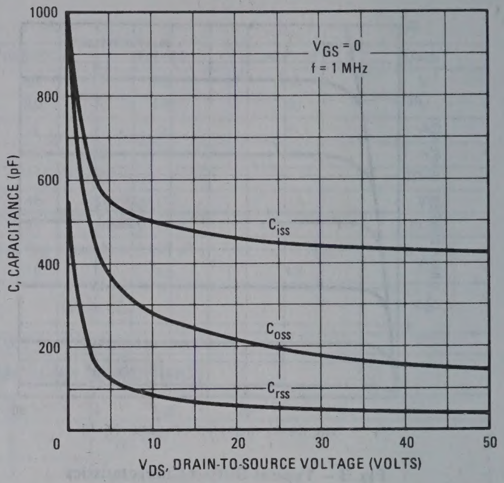


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

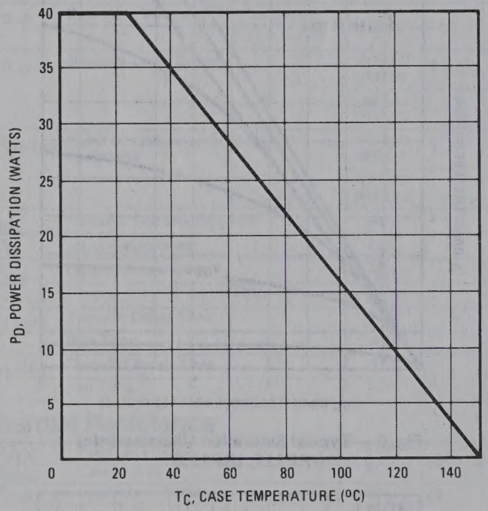


Fig. 11 — Power Vs. Temperature Derating

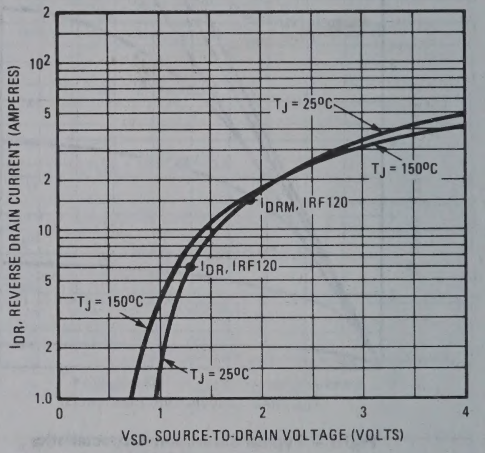


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

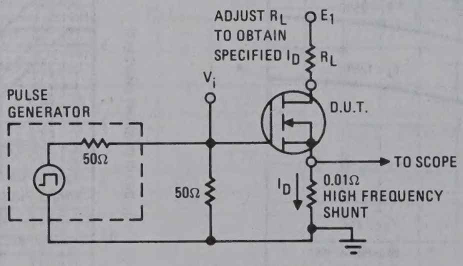
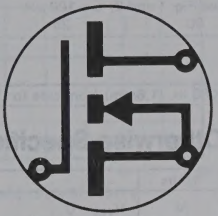


Fig. 13 — Switching Time Test Circuit

PD-9.303

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF130 IRF131 IRF132 IRF133



N Channel

100 Volt, 0.18 Ohm HEXFET™

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They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

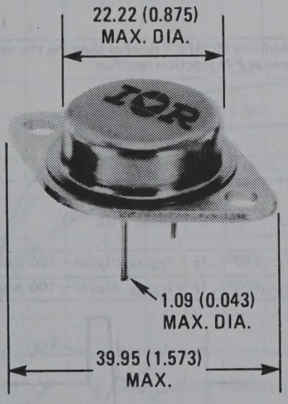
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

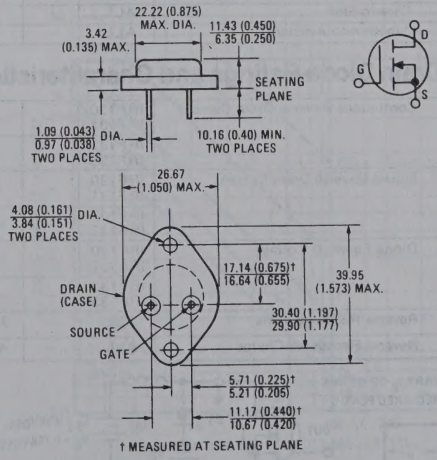
Product Summary

Part Number	V_{DS}	R_{D} (on)	I_D
IRF130	100V	0.18Ω	12A
IRF131	60V	0.18Ω	12A
IRF132	100V	0.25Ω	10A
IRF133	60V	0.25Ω	10A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings

Parameter		IRF130	IRF131	IRF132	IRF133	Units
V_{DS}	Drain — Source Voltage	100	60	100	60	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	100	60	100	60	V
I_D @ $T_C \cong 91.0^oC$	Continuous Drain Current	12	12	10	10	A
I_{DM}	Pulsed Drain Current	30	30	25	25	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	75 (See Fig. 11)				W
	Linear Derating Factor	0.6 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 30	30	25	25	A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10 sec)				^oC

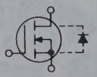
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF130 IRF132	100	—	—	V	$V_{GS} = 0$
		IRF131 IRF133	60	—	—	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	0.1	1.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0$
			—	0.2	4.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_J = 125^oC$
$I_{D\ (on)}$	On-State Drain Current	IRF130 IRF131	14	—	—	A	V_{DS} = 25V, V_{GS} = 10V
		IRF132 IRF133	12	—	—	A	
$R_{DS\ (on)}$	Static Drain-Source On State Resistance	IRF130 IRF131	—	0.14	0.18	Ω	V_{GS} = 10V, I_D = 6A
		IRF132 IRF133	—	0.20	0.25	Ω	
g_{fs}	Forward Transconductance	ALL	3.0	5.0	—	S (℧)	V_{DS} = 25V, I_D = 6A
C_{iss}	Input Capacitance	ALL	—	700	900	pF	$V_{GS} = 0$, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	150	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	—	30	50	ns	V_{DS} = 25V, I_D = 8A (See Fig. 13) $T_J = 125^oC$ (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	80	150	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	80	150	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	0.2	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF130 IRF131	—	—	12	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF132 IRF133	—	—	10		
I_{DRM}	Pulsed Reverse Drain Current	IRF130 IRF131	—	—	30	A	
		IRF132 IRF133	—	—	25		
V_{SD}	Diode Forward Voltage	IRF130 IRF131	—	—	2.0	V	$T_J = 25^oC$, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF132 IRF133	—	—	1.8	V	
t_{rr}	Reverse Recovery Time	ALL	—	300	—	ns	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.0	—	μC	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

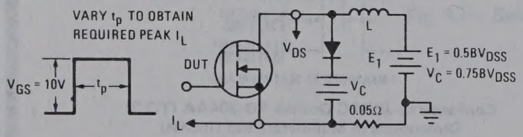


Fig. 1 — Clamped Inductive Test Circuit

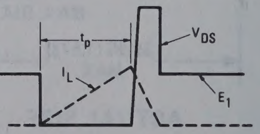


Fig. 2 — Clamped Inductive Waveforms

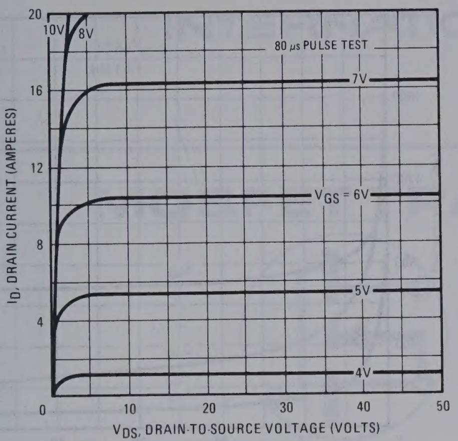


Fig. 3 – Typical Output Characteristics

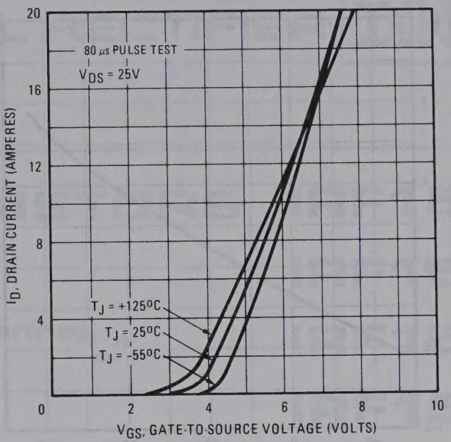


Fig. 4 – Typical Transfer Characteristics

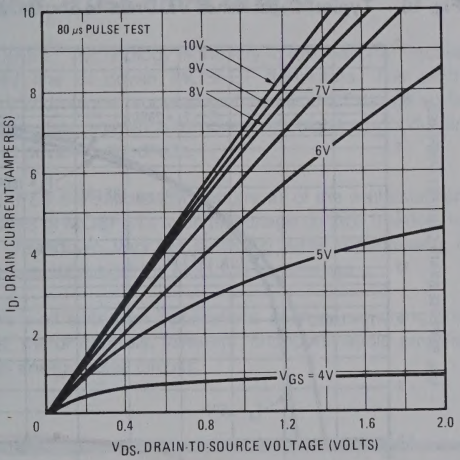


Fig. 5 – Typical Saturation Characteristics (IRF130, IRF131)

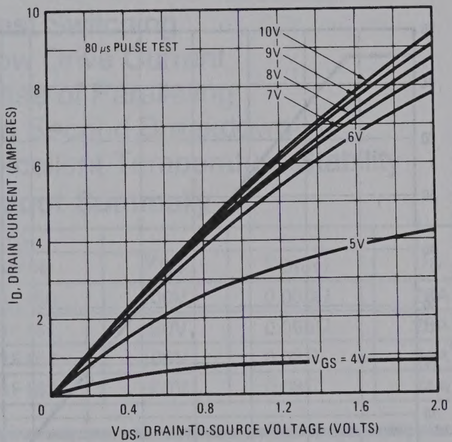


Fig. 6 – Typical Saturation Characteristics (IRF132, IRF133)

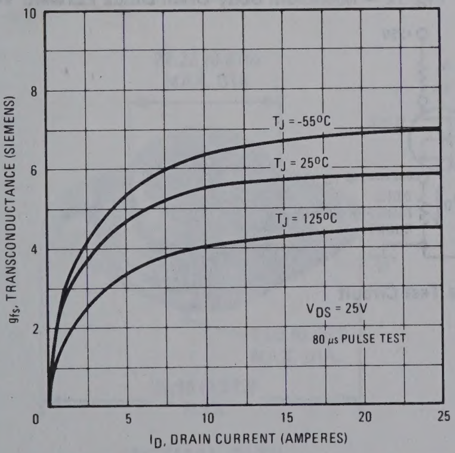


Fig 7. – Typical Transconductance Vs. Drain Current

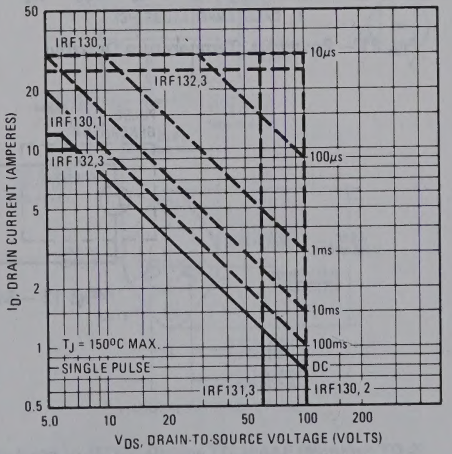


Fig. 8 – Maximum Safe Operating Area

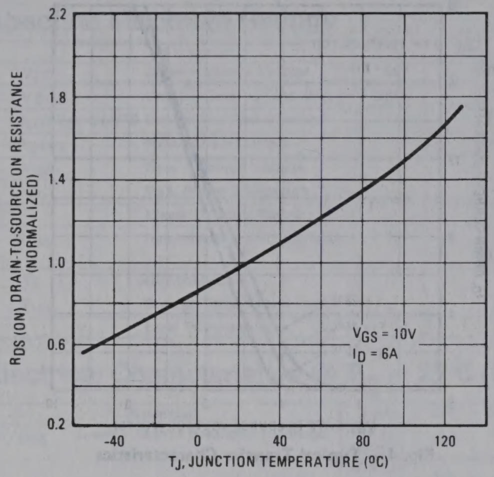


Fig. 9 – Normalized On-Resistance Vs. Temperature

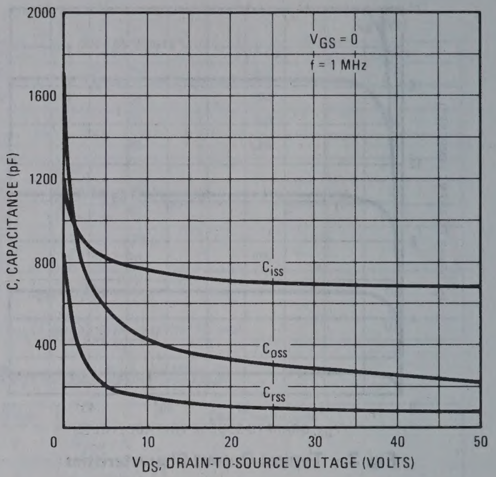


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

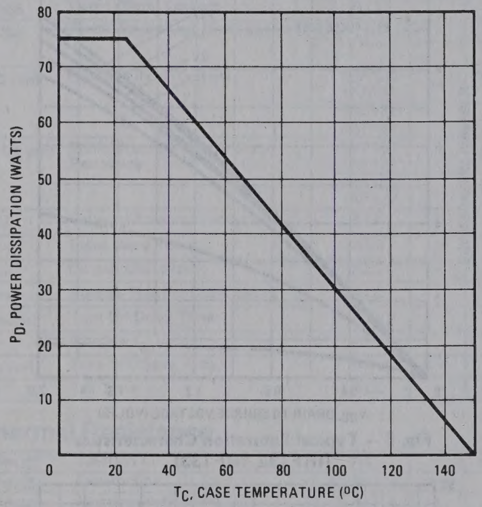


Fig. 11 – Power Vs. Temperature Derating

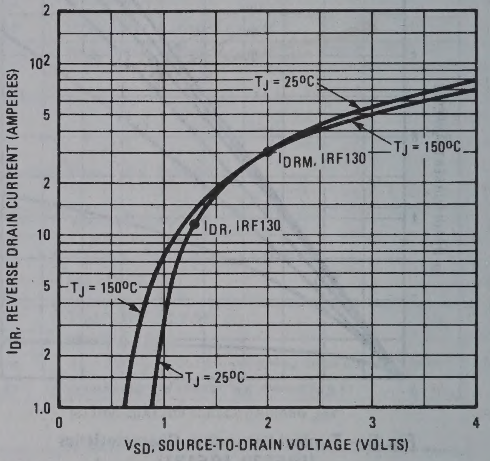


Fig. 12 – Maximum Body-Drain Diode Forward Voltage

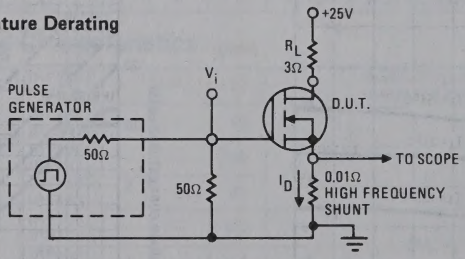
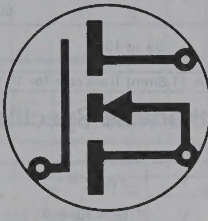


Fig. 13 – Switching Time Test Circuit

PD-9.305

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF150 IRF151 IRF152 IRF153



N Channel

100 Volt, 0.055 Ohm HEXFET™

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

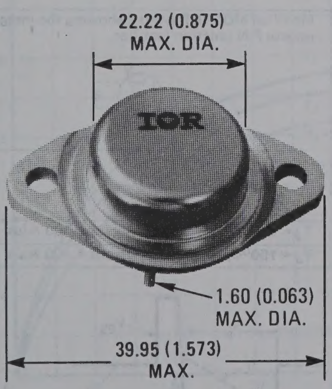
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

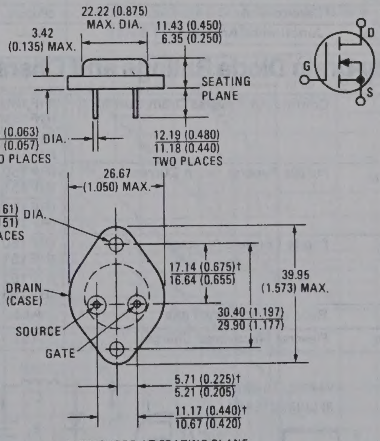
Product Summary

Part Number	V_{DS}	$R_{D(on)}$	I_D
IRF150	100V	0.055Ω	28A
IRF151	60V	0.055Ω	28A
IRF152	100V	0.08Ω	24A
IRF153	60V	0.08Ω	24A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Conforms to JEDEC Outline TO-204AE (Modified TO-3)
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings

Parameter		IRF150	IRF151	IRF152	IRF153	Units
V_{DS}	Drain — Source Voltage	100	60	100	60	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	100	60	100	60	V
I_D @ $T_C \cong 94.0^\circ C$	Continuous Drain Current	28		24		A
I_{DM}	Pulsed Drain Current	70		60		A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	150 (See Fig. 11)				W
	Linear Derating Factor	1.2 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 µH 70		60		A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10 sec)				°C

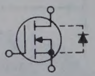
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF150 IRF152	100	—	—	V	$V_{GS} = 0$
		IRF151 IRF153	60	—	—	V	$I_D = 1.0$ mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	100	nA	$V_{GS} = 20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	0.1	1.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0$
			—	0.2	4.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_J = 125^\circ C$
I_D (on)	On-State Drain Current	IRF150 IRF151	40	—	—	A	$V_{DS} = 25V$, $V_{GS} = 10V$
		IRF152 IRF153	33	—	—	A	
R_{DS} (on)	Static Drain-Source On State Resistance	IRF150 IRF151	—	0.045	0.055	Ω	$V_{GS} = 10V$, $I_D = 14A$
		IRF152 IRF153	—	0.06	0.08	Ω	
g_{fs}	Forward Transconductance	ALL	6	10	—	S (℧)	$V_{DS} = 25V$, $I_D = 14A$
C_{iss}	Input Capacitance	ALL	—	3000	4000	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	—	1000	1500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	350	500	pF	
t_d (on)	Turn-On Delay Time	ALL	—	40	60	ns	$I_D = 14A$, $E_1 = 0.5\ BV_{DSS}$ (See Fig. 13) $T_J = 125^\circ C$ (MOSFET Switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	150	200	ns	
t_d (off)	Turn-Off Delay Time	ALL	—	200	300	ns	
t_f	Fall Time	ALL	—	150	200	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	0.83	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	0.2	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF150 IRF151	—	—	28	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF152 IRF153	—	—	24		
I_{DRM}	Pulsed Reverse Drain Current	IRF150 IRF151	—	—	70	A	
		IRF152 IRF153	—	—	60		
V_{SD}	Diode Forward Voltage	IRF150 IRF151	—	—	1.7	V	$T_J = 25^\circ C$, $I_F = I_{DRM}$, $V_{GS} = 0V$
		IRF152 IRF153	—	—	1.6	V	
t_{rr}	Reverse Recovery Time	ALL	—	500	—	ns	$T_J = 150^\circ C$, $I_F = I_{DRM}$, $dI_F/dt = 100$ A/µs
Q_{RR}	Reverse Recovered Charge	ALL	—	10.0	—	µC	$T_J = 150^\circ C$, $I_F = I_{DRM}$, $dI_F/dt = 100$ A/µs

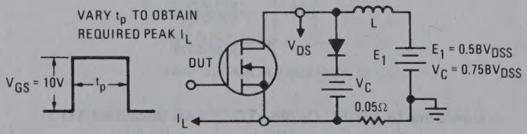


Fig. 1 — Clamped Inductive Test Circuit

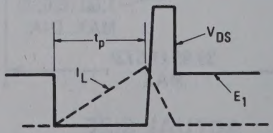


Fig. 2 — Clamped Inductive Waveforms

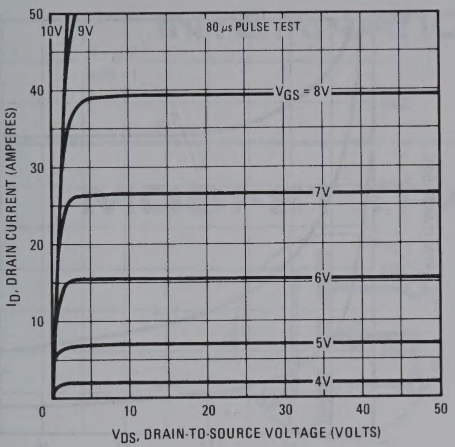


Fig. 3 — Typical Output Characteristics

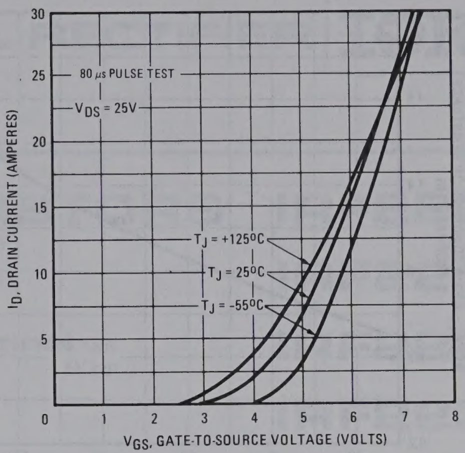


Fig. 4 — Typical Transfer Characteristics

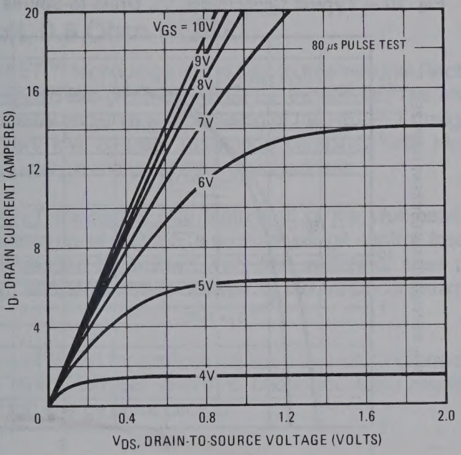


Fig. 5 — Typical Saturation Characteristics (IRF150, IRF151)

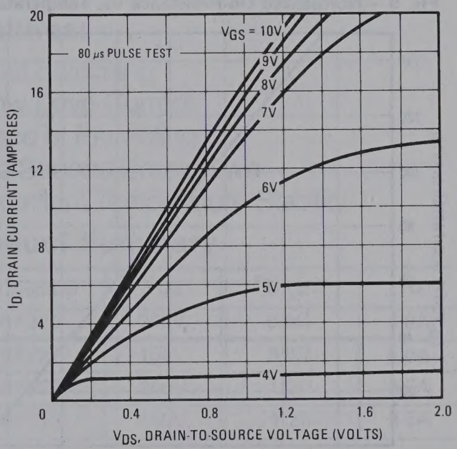


Fig. 6 — Typical Saturation Characteristics (IRF152, IRF153)

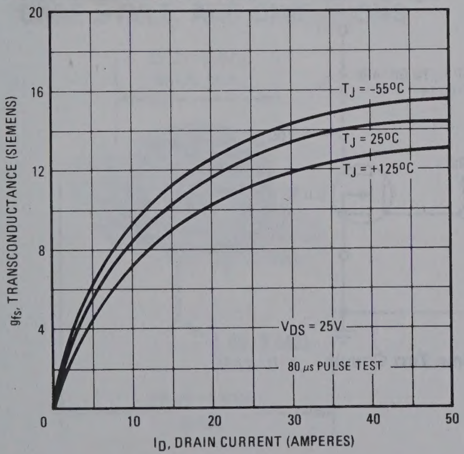


Fig 7. — Typical Transconductance Vs. Drain Current

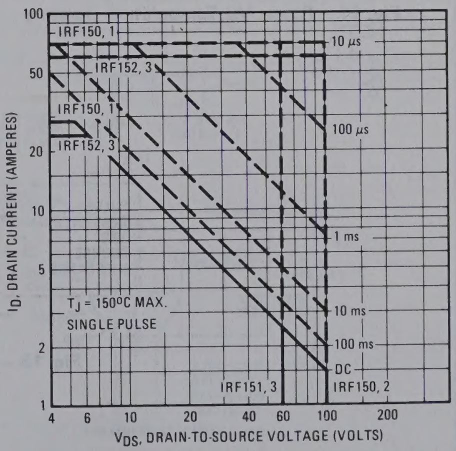


Fig. 8 — Maximum Safe Operating Area

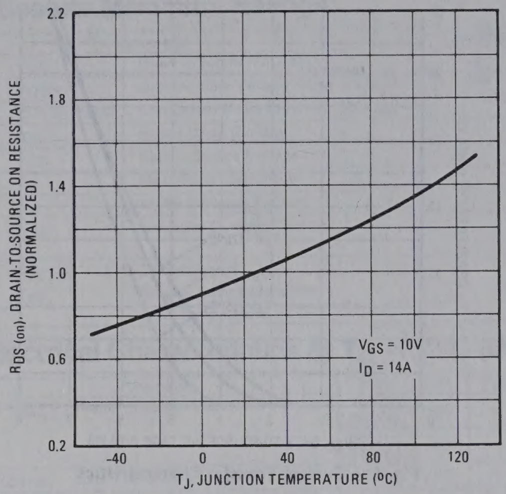


Fig. 9 – Normalized On-Resistance Vs. Temperature

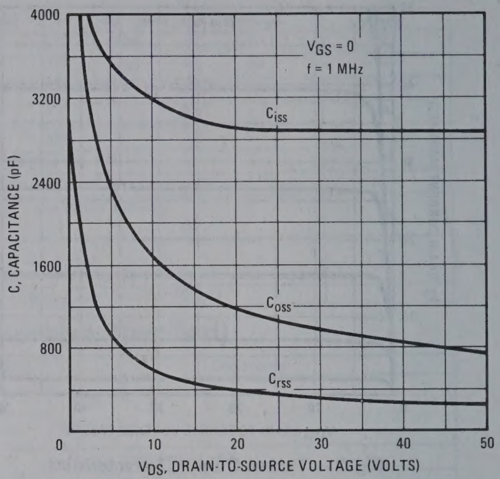


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

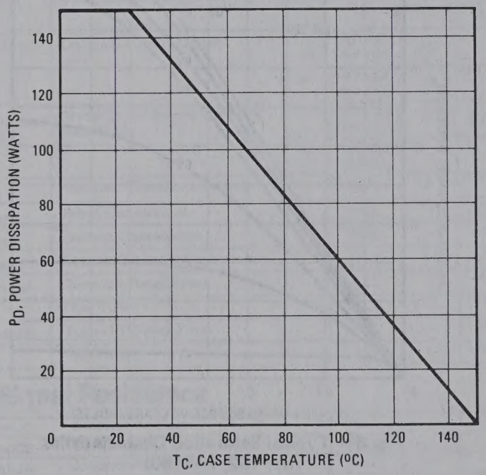


Fig. 11 – Power Vs. Temperature Derating

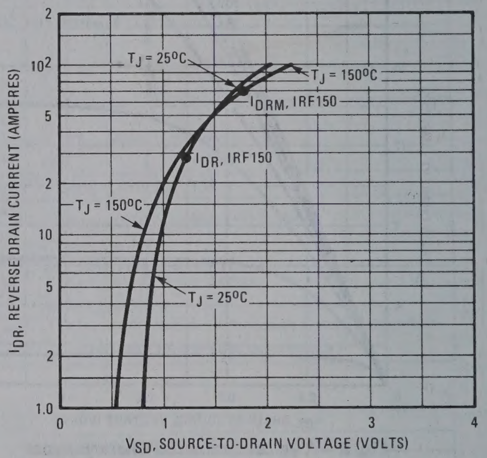


Fig. 12 – Maximum Body-Drain Diode Forward Voltage

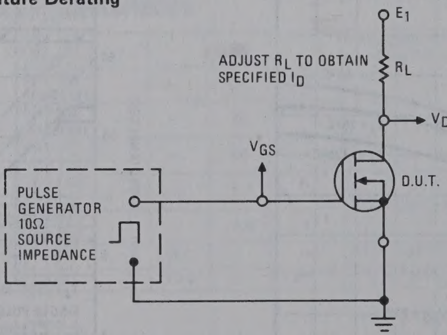
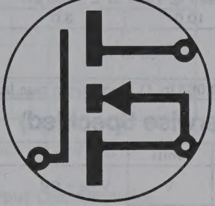

E_1
ADJUST R_L TO OBTAIN SPECIFIED I_D
R_L
V_{DS}
V_{GS}
D.U.T.
PULSE GENERATOR 10Ω SOURCE IMPEDANCE

Fig. 13 – Switching Time Test Circuit

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF220 IRF221 IRF222 IRF223



N Channel

200 Volt, 0.8 Ohm HEXFET™

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

Features:

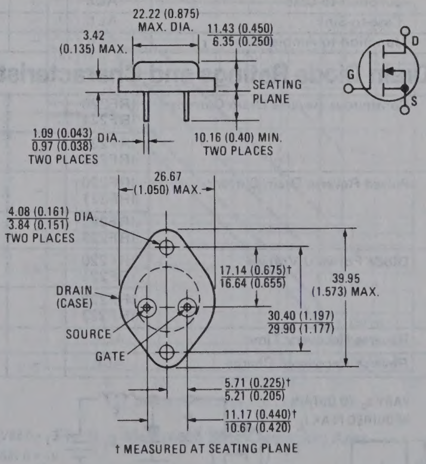
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{D\ (on)}$	I_D
IRF220	200V	0.8Ω	4.0A
IRF221	150V	0.8Ω	4.0A
IRF222	200V	1.2Ω	3.5A
IRF223	150V	1.2Ω	3.5A

CASE STYLE AND DIMENSIONS

ACTUAL SIZE



Conforms to JEDEC Outline TO-204AA (TO-3)

Dimensions in Millimeters and (Inches)

IRF220, IRF221, IRF222, IRF223 Devices

Absolute Maximum Ratings

	Parameter	IRF220	IRF221	IRF222	IRF223	Units
V_{DS}	Drain – Source Voltage	200	150	200	150	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	200	150	200	150	V
I_D @ $T_C \cong 89.5^oC$	Continuous Drain Current	4.0	4.0	3.5	3.5	A
I_{DM}	Pulsed Drain Current	10.0	10.0	8.0	8.0	A
V_{GS}	Gate – Source Voltage	±20				V
P_D	Max. Power Dissipation	40 (See Fig. 11)				W
	Linear Derating Factor	0.32 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 10.0	10.0	8.0	8.0	A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				^oC

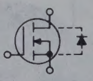
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRF220 IRF222	200	–	–	V	V_{GS} = 0V
		IRF221 IRF223	150	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate – Body Leakage	ALL	–	–	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0	mA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	0.2	4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0V, $T_J = 125^oC$
I_D (on)	On-State Drain Current	IRF220 IRF221	5.0	–	–	A	V_{DS} = 25V, V_{GS} = 10V
		IRF222 IRF223	4.0	–	–	A	
R_{DS} (on)	Static Drain-Source On State Resistance	IRF220 IRF221	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.0A
		IRF222 IRF223	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance	ALL	1.3	2.3	–	S (℧)	V_{DS} = 25V, I_D = 2.0A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
t_d (on)	Turn-On Delay Time	ALL	–	20	40	ns	I_D = 2A, E_1 = 0.5 BV_{DSS} (See Fig. 13) $T_J = 125^oC$ (MOSFET Switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
t_d (off)	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	–	0.2	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF220 IRF221	–	–	4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF222 IRF223	–	–	3.5		
I_{DRM}	Pulsed Reverse Drain Current	IRF220 IRF221	–	–	10.0	A	
		IRF222 IRF223	–	–	8.0		
V_{SD}	Diode Forward Voltage	IRF220 IRF221	–	–	1.57	V	$T_J = 25^oC$, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF222 IRF223	–	–	1.44	V	
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	6.0	–	μC	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

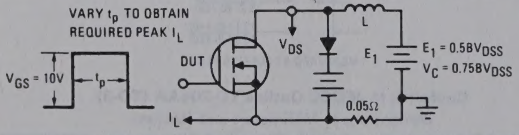


Fig. 1 – Clamped Inductive Test Circuit

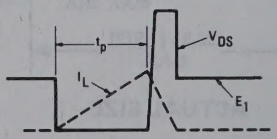


Fig. 2 – Clamped Inductive Waveforms

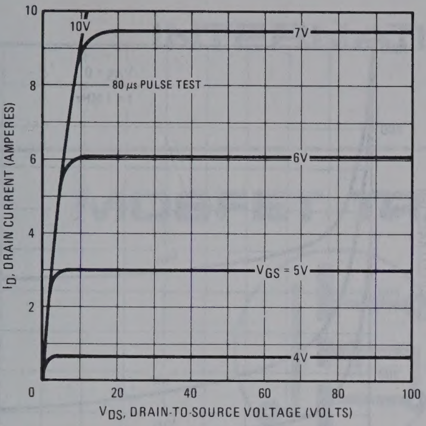


Fig. 3 — Typical Output Characteristics

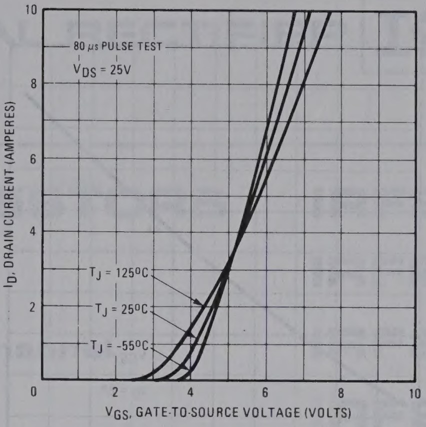


Fig. 4 — Typical Transfer Characteristics

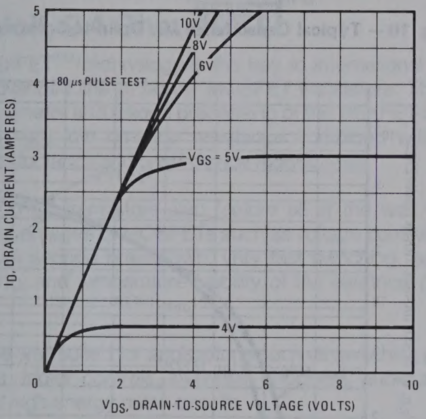


Fig. 5 — Typical Saturation Characteristics (IRF220, IRF221)

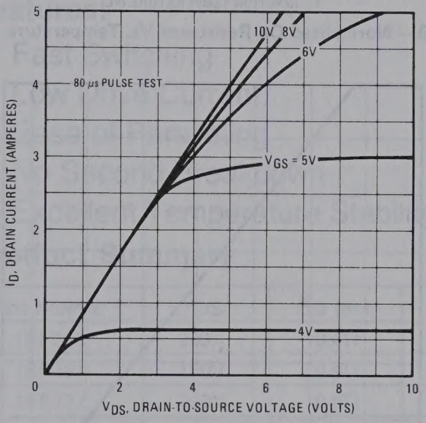


Fig. 6 — Typical Saturation Characteristics (IRF222, IRF223)

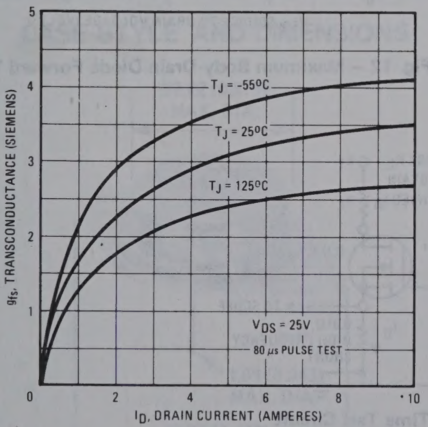


Fig 7. — Typical Transconductance Vs. Drain Current

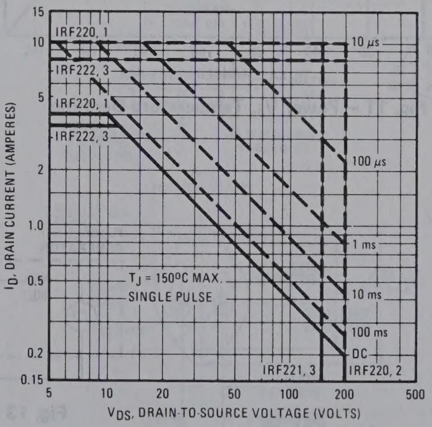


Fig. 8 — Maximum Safe Operating Area

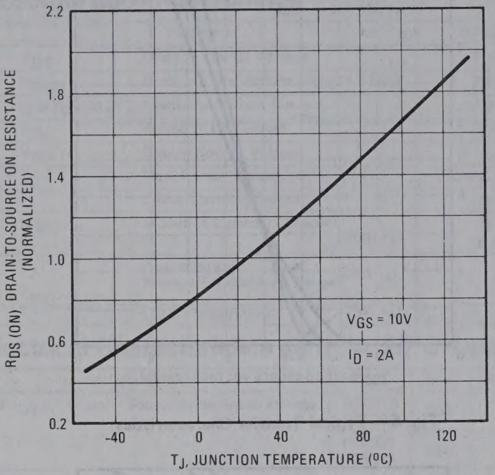


Fig. 9 — Normalized On-Resistance Vs. Temperature

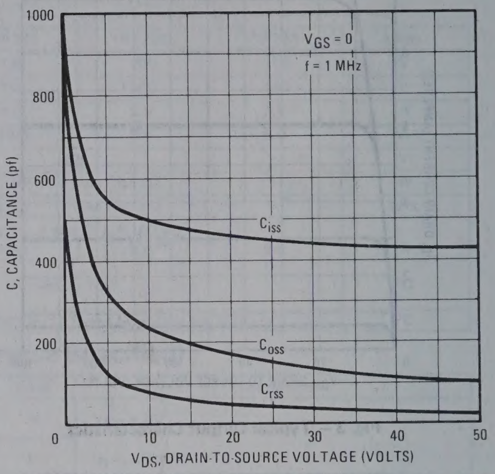


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

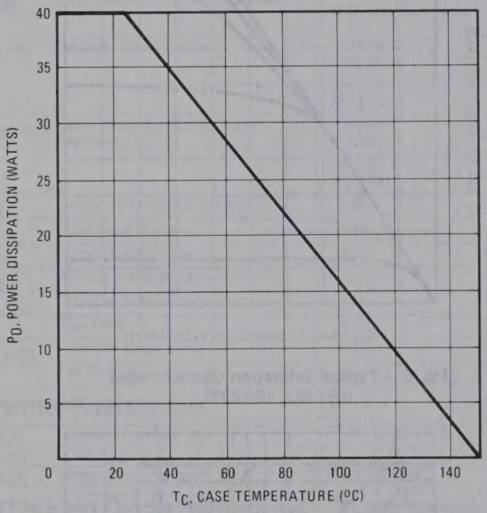


Fig. 11 — Power Vs. Temperature Derating

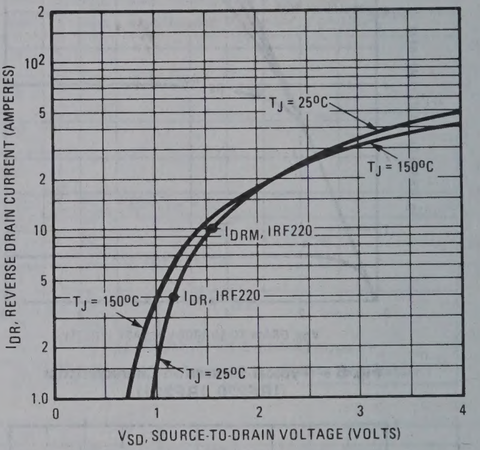


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

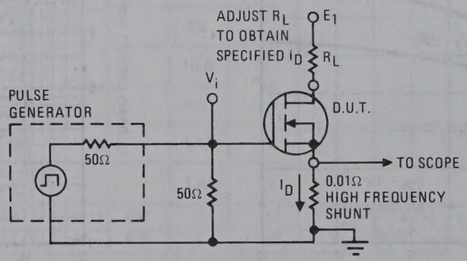
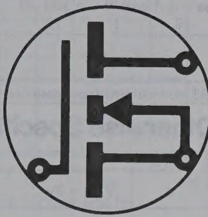

ADJUST R_L TO OBTAIN SPECIFIED I_D
E_1
R_L
V_i
PULSE GENERATOR
50Ω
50Ω
D.U.T.
TO SCOPE
I_D
0.01Ω HIGH FREQUENCY SHUNT

Fig. 13 — Switching Time Test Circuit

INTERNATIONAL RECTIFIER **IOR**

MOSFET TRANSISTORS IRF230 IRF231 IRF232 IRF233



N Channel

200 Volt, 0.4 Ohm HEXFET™

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

Features:

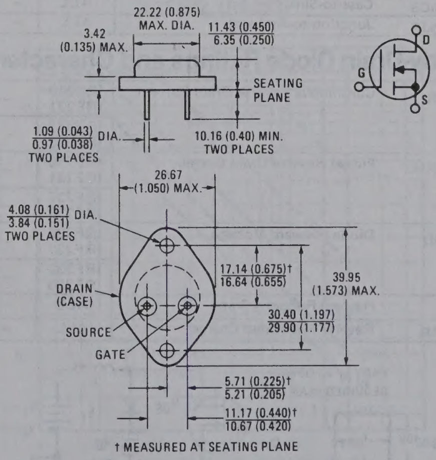
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	R_{D} (on)	I_D
IRF230	200V	0.4Ω	7A
IRF231	150V	0.4Ω	7A
IRF232	200V	0.6Ω	6A
IRF233	150V	0.6Ω	6A

CASE STYLE AND DIMENSIONS

ACTUAL SIZE



Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

IRF230, IRF231, IRF232, IRF233 Devices

Absolute Maximum Ratings

Parameter		IRF230	IRF231	IRF232	IRF233	Units
V_{DS}	Drain — Source Voltage	200	150	200	150	V
V_{DGR}	Drain — Gate Voltage ($R_{GS} = 1\ M\Omega$)	200	150	200	150	V
$I_D @ T_C \cong 91.0^oC$	Continuous Drain Current	7	7	6	6	A
I_{DM}	Pulsed Drain Current	15	15	12	12	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	75 (See Fig. 11)				W
	Linear Derating Factor	0.6 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) $L = 100\ \mu H$ 15	15	12	12	A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10 sec.				^oC

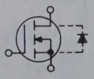
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF230 IRF232	200	—	—	V	$V_{GS} = 0V$
		IRF231 IRF233	150	—	—	V	$I_D = 1.0\ mA$
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 1\ mA$
I_{GSS}	Gate — Body Leakage	ALL	—	—	100	nA	$V_{GS} = 20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	0.1	1.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0V$
			—	0.2	4.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0V$, $T_J = 125^oC$
I_D (on)	On-State Drain Current	IRF230 IRF231	9.0	—	—	A	$V_{DS} = 25V, V_{GS} = 10V$
		IRF232 IRF233	8.0	—	—	A	
R_{DS} (on)	Static Drain-Source On State Resistance	IRF230 IRF231	—	0.25	0.4	Ω	$V_{GS} = 10V, I_D = 3.5A$
		IRF232 IRF233		0.4	0.6	Ω	
g_{fs}	Forward Transconductance	ALL	2.5	4.5	—	S (℧)	$V_{DS} = 25V, I_D = 3.5A$
C_{iss}	Input Capacitance	ALL	—	700	900	pF	$V_{GS} = 0V, V_{DS} = 25V$, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	—	250	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	80	150	pF	
t_d (on)	Turn-On Delay Time	ALL	—	30	50	ns	$I_D = 4A, E_1 = 0.5\ BV_{DSS}$ (See Fig. 13) $T_J = 125^oC$ (MOSFET Switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	70	140	ns	
t_d (off)	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	70	140	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	0.2	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF230 IRF231	—	—	7	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF232 IRF233	—	—	6		
I_{DRM}	Pulsed Reverse Drain Current	IRF230 IRF231	—	—	15	A	
		IRF232 IRF233	—	—	12		
V_{SD}	Diode Forward Voltage	IRF230 IRF231	—	—	1.45	V	$T_J = 25^oC, I_F = I_{DRM}, V_{GS} = 0V$
		IRF232 IRF233	—	—	1.31	V	
t_{rr}	Reverse Recovery Time	ALL	—	650	—	ns	$T_J = 150^oC, I_F = I_{DRM}, dI_F/dt = 100\ A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	10.0	—	μC	$T_J = 150^oC, I_F = I_{DRM}, dI_F/dt = 100\ A/\mu s$

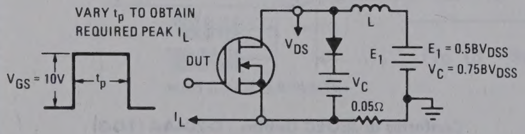


Fig. 1 — Clamped Inductive Test Circuit

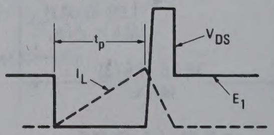


Fig. 2 — Clamped Inductive Waveforms

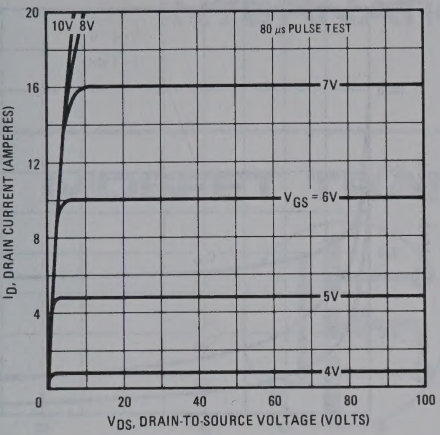


Fig. 3 — Typical Output Characteristics

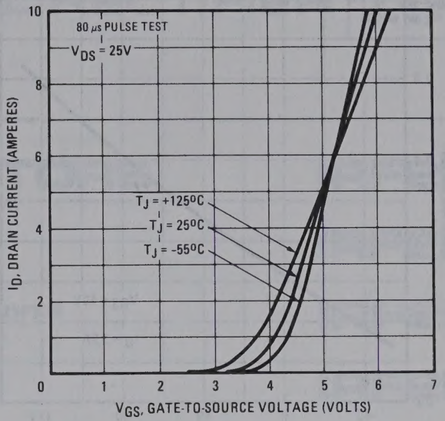


Fig. 4 — Typical Transfer Characteristics

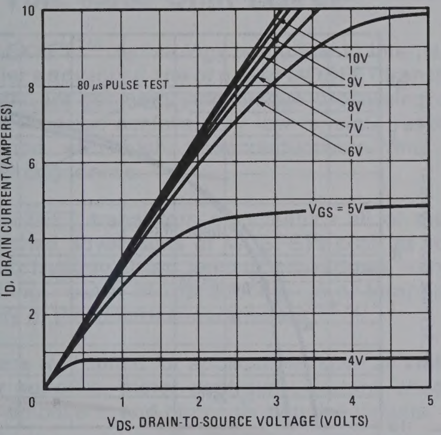


Fig. 5 — Typical Saturation Characteristics (IRF230, IRF231)

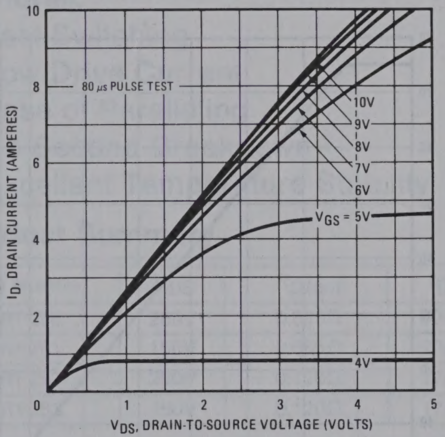


Fig. 6 — Typical Saturation Characteristics (IRF232, IRF233)

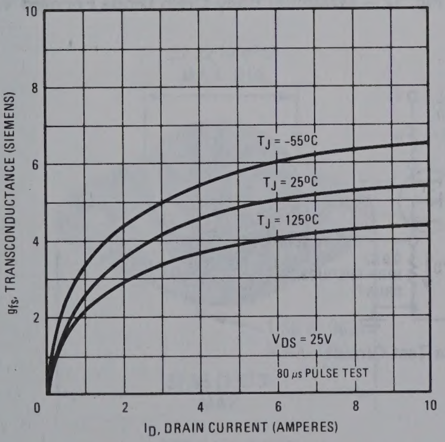


Fig 7. — Typical Transconductance Vs. Drain Current

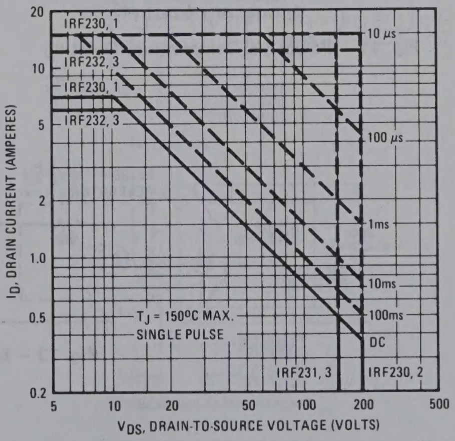


Fig. 8 — Maximum Safe Operating Area

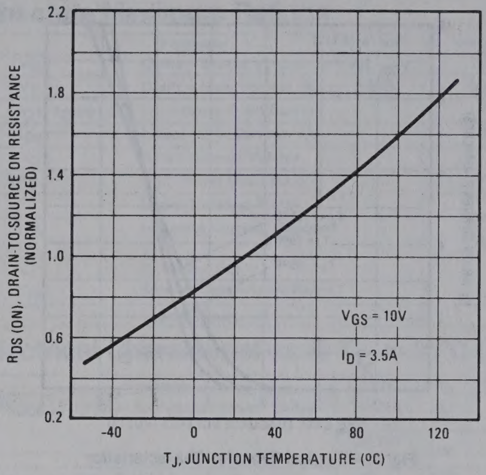


Fig. 9 — Normalized On-Resistance Vs. Temperature

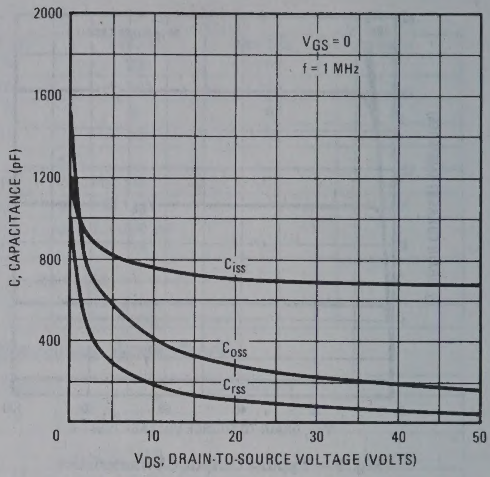


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

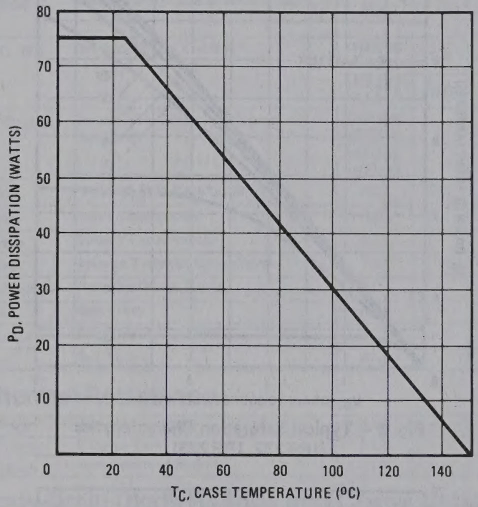


Fig. 11 — Power Vs. Temperature Derating

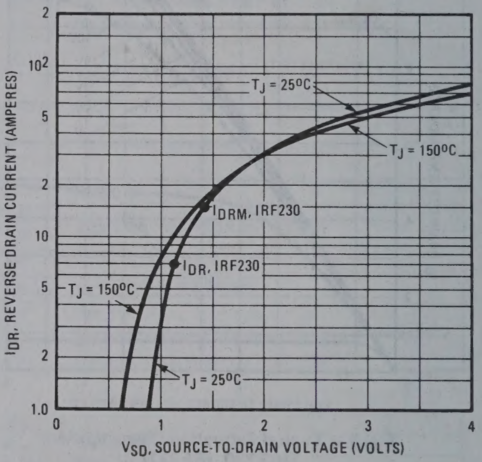


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

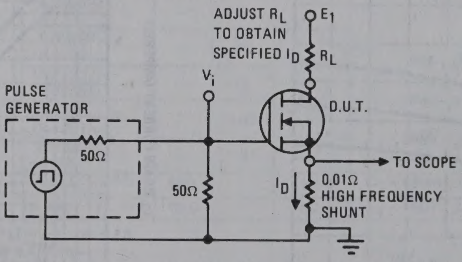
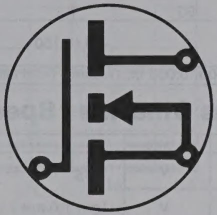

ADJUST R_L TO OBTAIN SPECIFIED I_D
E_1
R_L
V_i
PULSE GENERATOR
50Ω
50Ω
D.U.T.
TO SCOPE
I_D
0.01Ω HIGH FREQUENCY SHUNT

Fig. 13 — Switching Time Test Circuit

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS



IRF250
IRF251
IRF252
IRF253

200 Volt, 0.085 Ohm HEXFET™

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

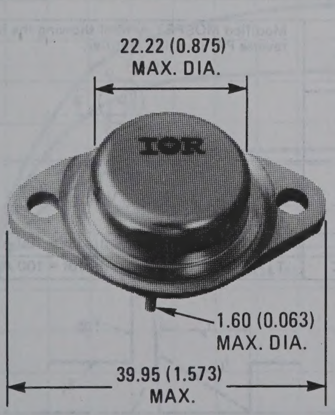
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

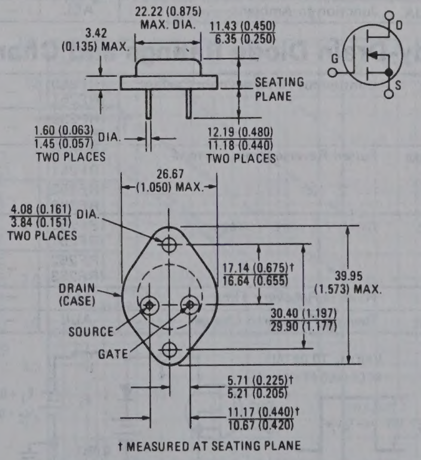
Product Summary

Part Number	V_{DS}	$R_{D(on)}$	I_D
IRF250	200V	0.085Ω	20A
IRF251	150V	0.085Ω	20A
IRF252	200V	0.120Ω	17A
IRF253	150V	0.120Ω	17A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Conforms to JEDEC Outline TO-204AE (Modified TO-3)
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings

	Parameter	IRF250	IRF251	IRF252	IRF253	Units
V_{DS}	Drain — Source Voltage	200	150	200	150	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	200	150	200	150	V
I_D @ $T_C \cong 94.0^oC$	Continuous Drain Current	20		17		A
I_{DM}	Pulsed Drain Current	60		50		A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	150 (See Fig. 11)				W
	Linear Derating Factor	1.2 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 60		50		A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				^oC

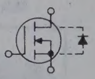
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF250 IRF252	200	—	—	V	V_{GS} = 0
		IRF251 IRF253	150	—	—	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	0.1	1.0	mA	V_{DS} = Max. Rating, V_{GS} = 0
			—	0.2	4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0, $T_J = 125^oC$
I_D (on)	On-State Drain Current	IRF250 IRF251	30	—	—	A	V_{DS} = 25V, V_{GS} = 10V
		IRF252 IRF253	25	—	—	A	
R_{DS} (on)	Static Drain-Source On State Resistance	IRF250 IRF251	—	0.07	0.085	Ω	V_{GS} = 10V, I_D = 10A
		IRF252 IRF253	—	0.09	0.120	Ω	
g_{fs}	Forward Transconductance	ALL	8	12	—	S (℧)	V_{DS} = 25V, I_D = 10A
C_{iss}	Input Capacitance	ALL	—	1800	3000	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	—	800	1200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	300	500	pF	
t_d (on)	Turn-On Delay Time	ALL	—	40	60	ns	I_D = 10A, E_1 = 0.5 BV_{DSS} (See Fig. 13) $T_J = 125^oC$ (MOSFET Switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	140	200	ns	
t_d (off)	Turn-Off Delay Time	ALL	—	150	250	ns	
t_f	Fall Time	ALL	—	140	200	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	0.83	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	0.2	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF250 IRF251	—	—	20	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF252 IRF253	—	—	17		
I_{DRM}	Pulsed Reverse Drain Current	IRF250 IRF251	—	—	60	A	
		IRF252 IRF253	—	—	50		
V_{SD}	Diode Forward Voltage	IRF250 IRF251	—	—	1.6	V	$T_J = 25^oC$, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF252 IRF253	—	—	1.5		
t_{rr}	Reverse Recovery Time	ALL	—	500	—	ns	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	10.0	—	μC	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

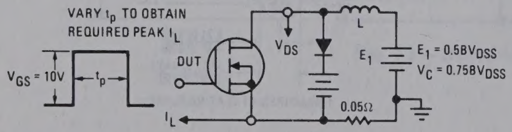


Fig. 1 — Clamped Inductive Test Circuit

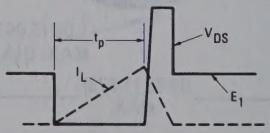


Fig. 2 — Clamped Inductive Waveforms

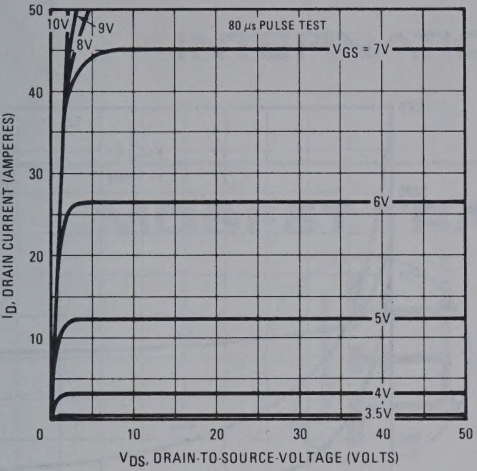


Fig. 3 — Typical Output Characteristics

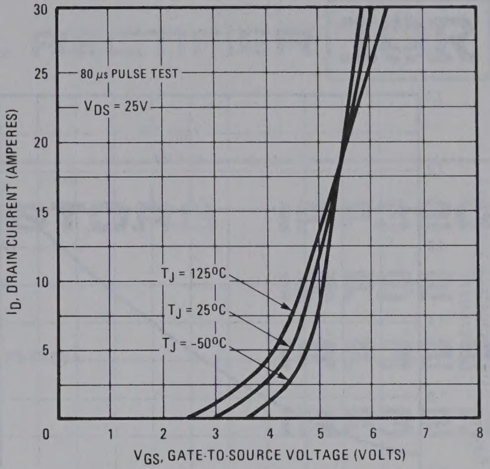


Fig. 4 — Typical Transfer Characteristics

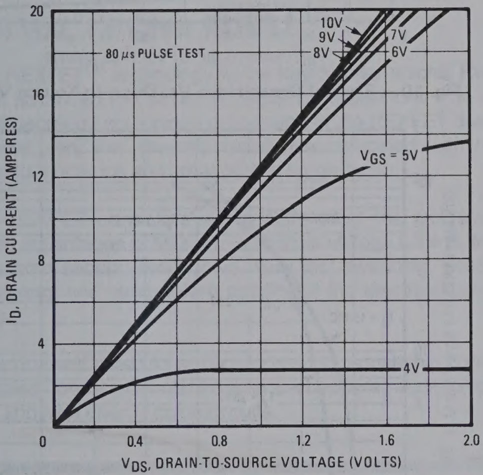


Fig. 5 — Typical Saturation Characteristics (IRF250, IRF251)

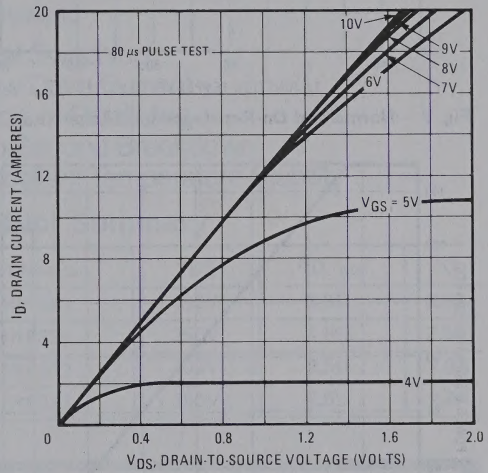


Fig. 6 — Typical Saturation Characteristics (IRF252, IRF253)

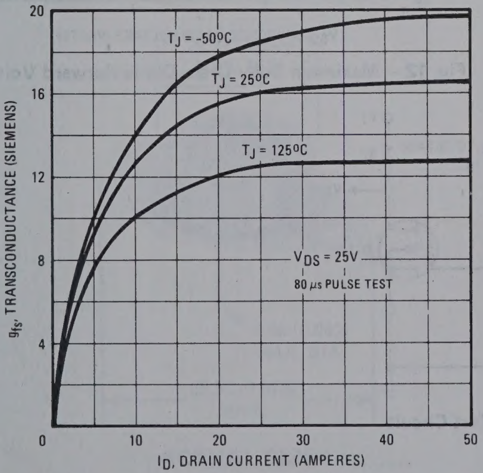


Fig. 7 — Typical Transconductance Vs. Drain Current

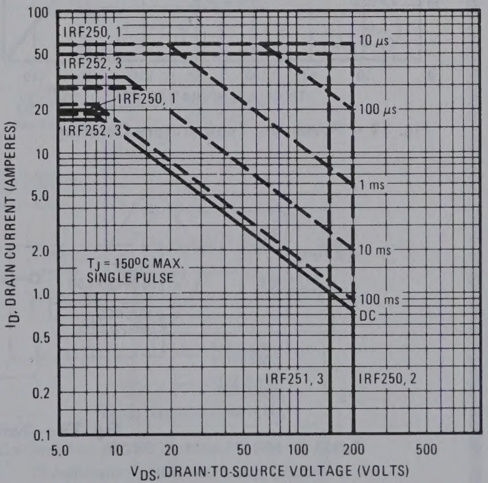


Fig. 8 — Maximum Safe Operating Area

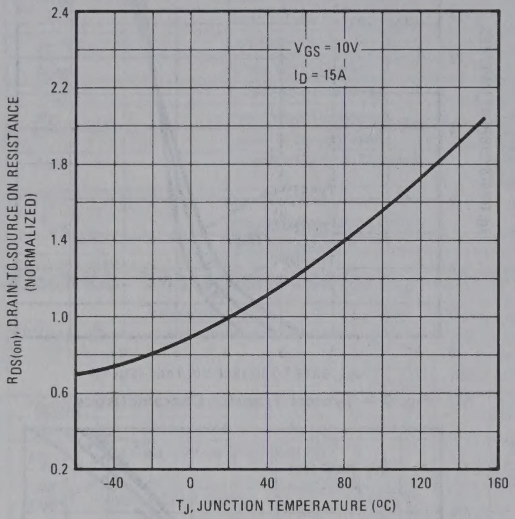


Fig. 9 – Normalized On-Resistance Vs. Temperature

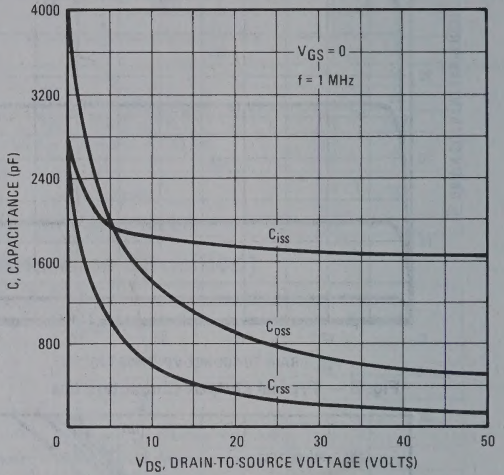


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

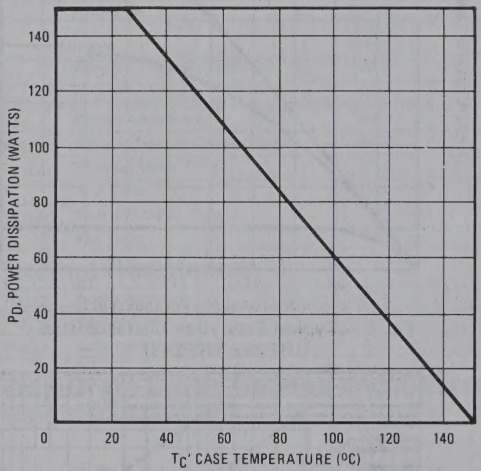


Fig. 11 – Power Vs. Temperature Derating

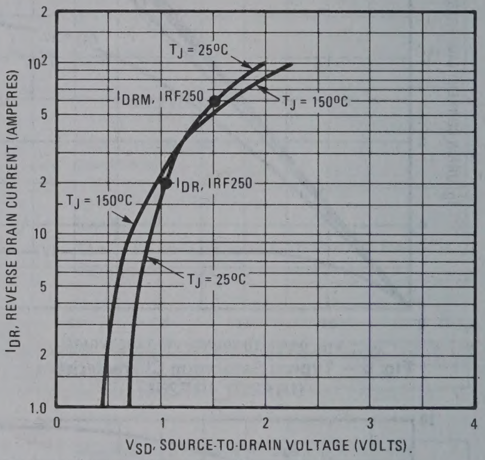


Fig. 12 – Maximum Body-Drain Diode Forward Voltage

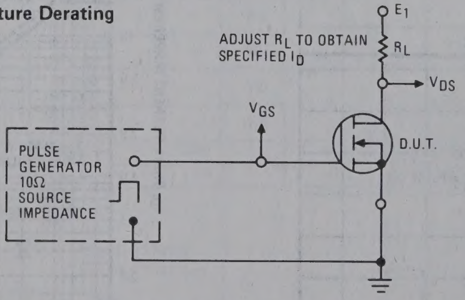
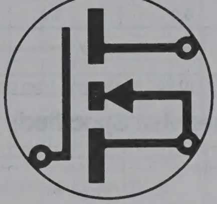

E_1
ADJUST R_L TO OBTAIN SPECIFIED I_D
R_L
V_{DS}
V_{GS}
D.U.T.
PULSE GENERATOR 10Ω SOURCE IMPEDANCE

Fig. 13 – Switching Time Test Circuit

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF320 IRF321 IRF322 IRF323



N Channel

400 Volt, 1.8 Ohm HEXFET™

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

Features:

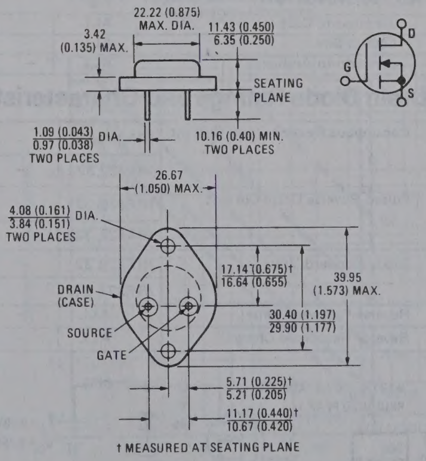
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{D\,(on)}$	I_D
IRF320	400V	1.8Ω	2.5A
IRF321	350V	1.8Ω	2.5A
IRF322	400V	2.5Ω	2.0A
IRF323	350V	2.5Ω	2.0A

CASE STYLE AND DIMENSIONS

ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)

Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings

	Parameter	IRF320	IRF321	IRF322	IRF323	Units
V_{DS}	Drain — Source Voltage	400	350	400	350	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	400	350	400	350	V
I_D @ $T_C \cong 89.5^oC$	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_{DM}	Pulsed Drain Current	6.0	6.0	5.0	5.0	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	40 (See Fig. 11)				W
	Linear Derating Factor	0.32 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH				A
		6.0	6.0	5.0	5.0	
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10 s)				°C

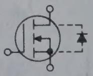
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF320 IRF322	400	—	—	V	$V_{GS} = 0$
		IRF321 IRF323	350	—	—	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	0.1	1.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0$
			—	0.2	4.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_J = 125^oC$
$I_{D\ (on)}$	On-State Drain Current	IRF320 IRF321	3.0	—	—	A	V_{DS} = 25V, V_{GS} = 10V
		IRF322 IRF323	2.5	—	—	A	
$R_{DS\ (on)}$	Static Drain-Source On State Resistance	IRF320 IRF321	—	1.5	1.8	Ω	V_{GS} = 10V, I_D = 1.5A
		IRF322 IRF323	—	1.8	2.5	Ω	
g_{fs}	Forward Transconductance	ALL	1.0	2.0	—	S (℧)	V_{DS} = 100V, I_D = 1.5A
C_{iss}	Input Capacitance	ALL	—	450	600	pF	$V_{GS} = 0$, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	—	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	40	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	—	20	40	ns	I_D = 1.5A, $E_1 = 0.5\ BV_{DSS}$ (See Fig. 13) $T_J = 125^oC$ (MOSFET Switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	25	50	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	25	50	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	0.2	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF320, 321	—	—	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF322, 323	—	—	2.0		
I_{DRM}	Pulsed Reverse Drain Current	IRF320, 321	—	—	6.0	A	
		IRF322, 323	—	—	5.0		
V_{SD}	Diode Forward Voltage	IRF320, 321	—	—	1.30	V	$T_J = 25^oC$, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF322, 323	—	—	1.25		
t_{rr}	Reverse Recovery Time	ALL	—	400	—	ns	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	5.0	—	μC	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

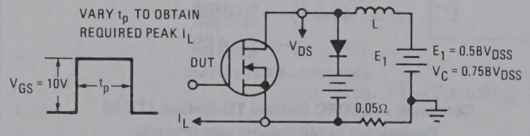


Fig. 1 — Clamped Inductive Test Circuit

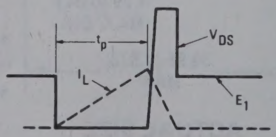


Fig. 2 — Clamped Inductive Waveforms

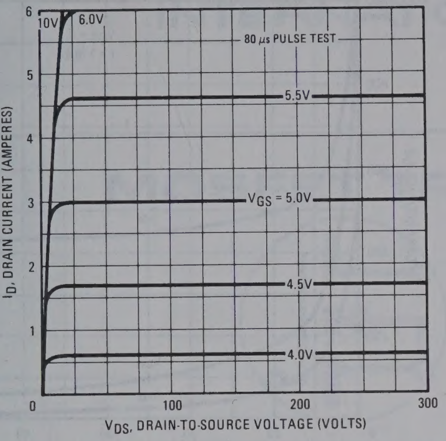


Fig. 3 — Typical Output Characteristics

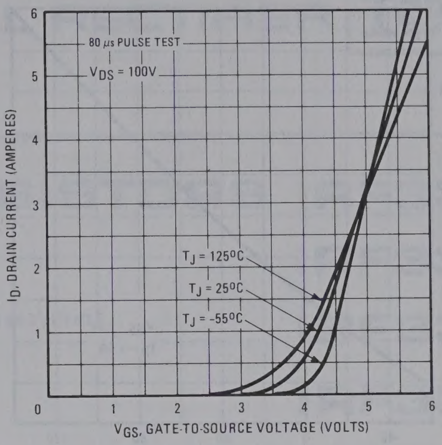


Fig. 4 — Typical Transfer Characteristics

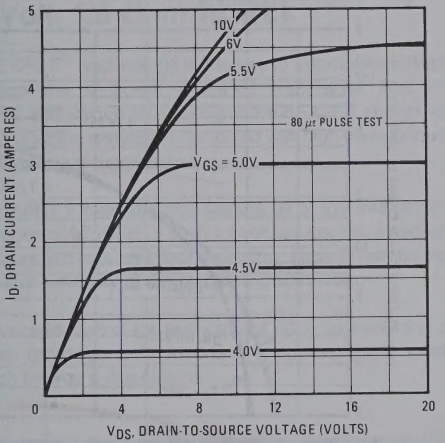


Fig. 5 — Typical Saturation Characteristics (IRF320, IRF321)

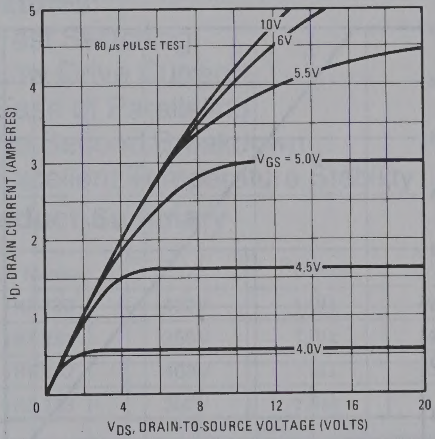


Fig. 6 — Typical Saturation Characteristics (IRF322, IRF323)

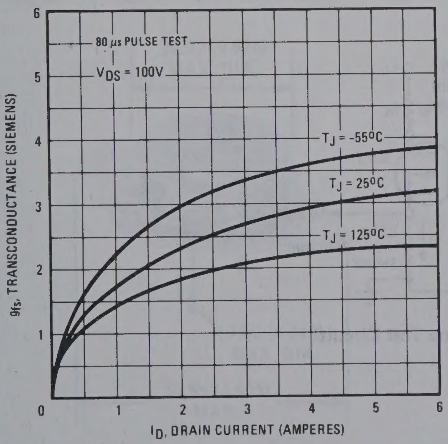


Fig. 7 — Typical Transconductance Vs. Drain Current

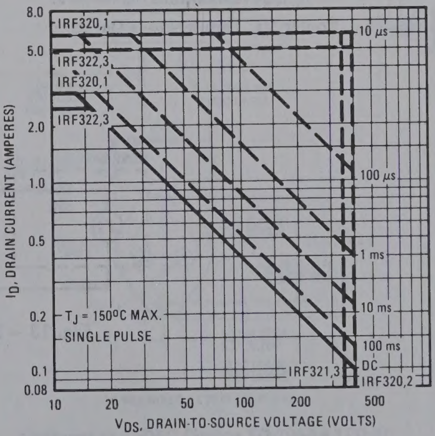


Fig. 8 — Maximum Safe Operating Area

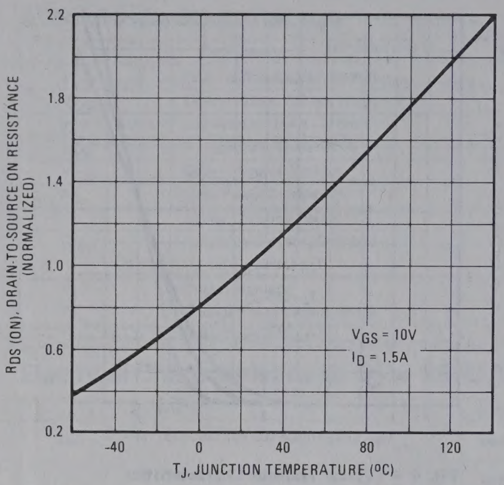


Fig. 9 — Normalized On-Resistance Vs. Temperature

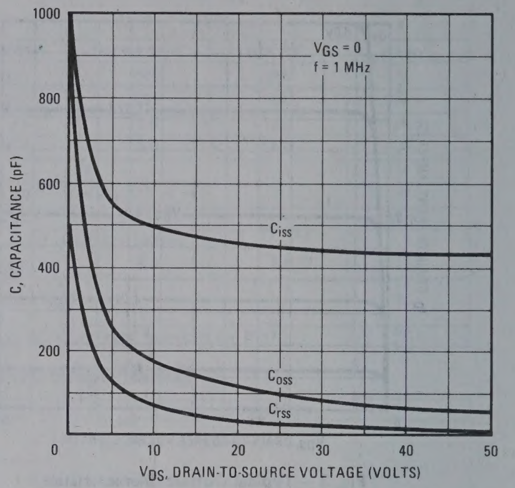


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

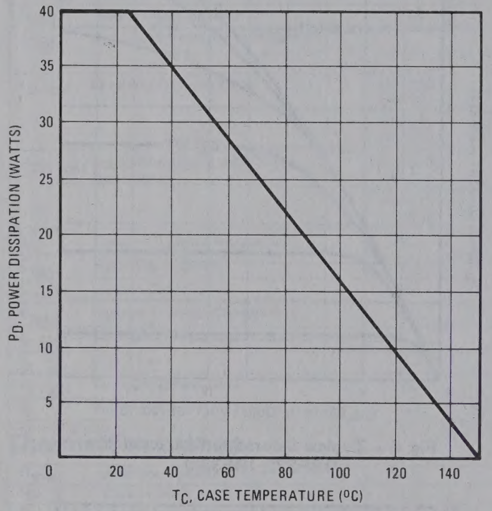


Fig. 11 — Power Vs. Temperature Derating

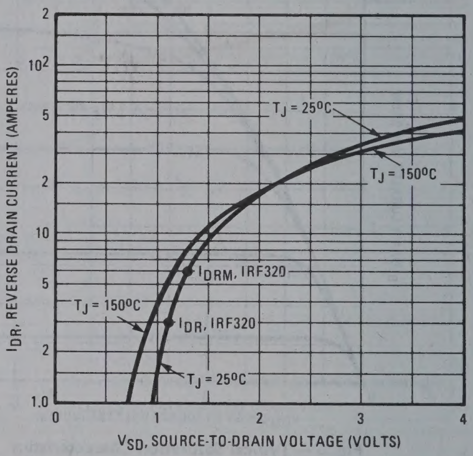


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

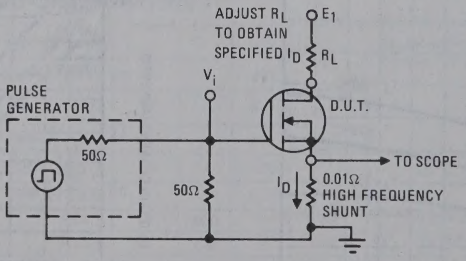
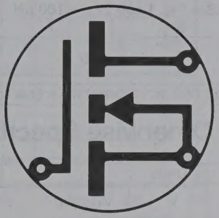

ADJUST R_L TO OBTAIN SPECIFIED I_D
E_1
R_L
V_i
PULSE GENERATOR
50Ω
D.U.T.
TO SCOPE
50Ω
I_D
0.01Ω HIGH FREQUENCY SHUNT

Fig. 13 — Switching Time Test Circuit

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF330 IRF331 IRF332 IRF333



N Channel

400 Volt, 1.0 Ohm HEXFET™

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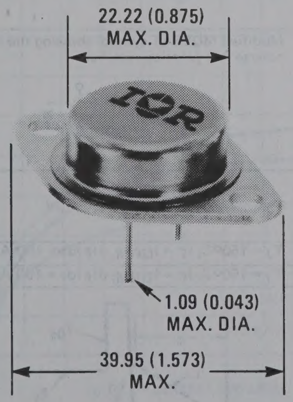
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

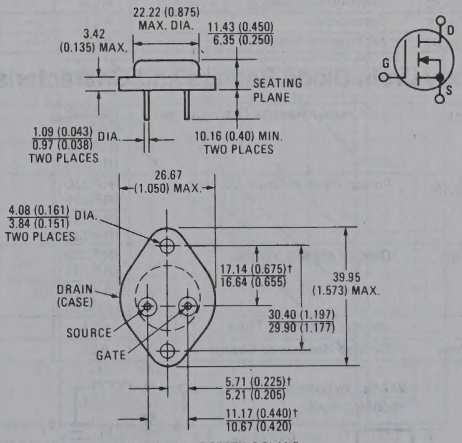
Product Summary

Part Number	V_{DS}	$R_{D\,(on)}$	I_D
IRF330	400V	1.0Ω	4A
IRF331	350V	1.0Ω	4A
IRF332	400V	1.5Ω	3.5A
IRF333	350V	1.5Ω	3.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings

Parameter		IRF330	IRF331	IRF332	IRF333	Units
V_{DS}	Drain – Source Voltage	400	350	400	350	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	400	350	400	350	V
I_D @ $T_C \cong 91.0^oC$	Continuous Drain Current	4	4	3.5	3.5	A
I_{DM}	Pulsed Drain Current	8	8	7	7	A
V_{GS}	Gate – Source Voltage	±20				V
P_D	Max. Power Dissipation	75 (See Fig. 11)				W
	Linear Derating Factor	0.6 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 8	8	7	7	A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10 sec)				^oC

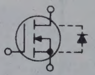
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRF330 IRF332	400	–	–	V	V_{GS} = 0
		IRF331 IRF333	350	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate – Body Leakage	ALL	–	–	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_J = 125°C
I_D (on)	On-State Drain Current	IRF330 IRF331	6.0	–	–	A	V_{DS} = 25V, V_{GS} = 10V
		IRF332 IRF333	5.0	–	–	A	
R_{DS} (on)	Static Drain-Source On State Resistance	IRF330 IRF331	–	0.8	1.0	Ω	V_{GS} = 10V, I_D = 2.0A
		IRF332 IRF333	–	1.0	1.5	Ω	
g_{fs}	Forward Transconductance	ALL	2.0	3.5	–	S (℧)	V_{DS} = 100V, I_D = 2A
C_{iss}	Input Capacitance	ALL	–	700	900	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
t_d (on)	Turn-On Delay Time	ALL	–	30	50	ns	V_{DS} = 25V, I_D = 2A (See Fig. 13) T_J = 125°C (MOSFET Switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	50	100	ns	
t_d (off)	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	50	100	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	–	0.2	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF330 IRF331	–	–	4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF332 IRF333	–	–	3.5		
I_{DRM}	Pulsed Reverse Drain Current	IRF330 IRF331	–	–	8.0	A	
		IRF332 IRF333	–	–	7.0		
V_{SD}	Diode Forward Voltage	IRF330 IRF331	–	–	1.15	V	T_J = 25°C, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF332 IRF333	–	–	1.13	V	
t_{rr}	Reverse Recovery Time	ALL	–	550	–	ns	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	8.0	–	μC	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

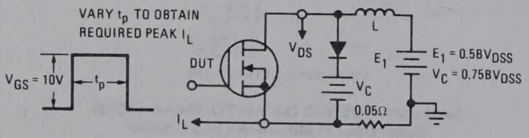


Fig. 1 – Clamped Inductive Test Circuit

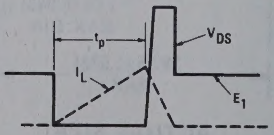


Fig. 2 – Clamped Inductive Waveforms

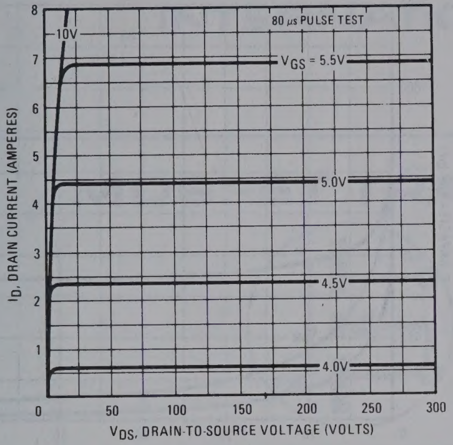


Fig. 3 — Typical Output Characteristics

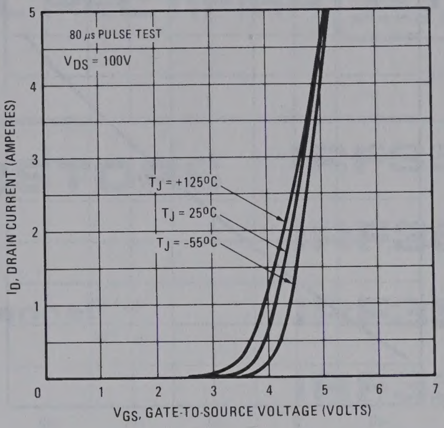


Fig. 4 — Typical Transfer Characteristics

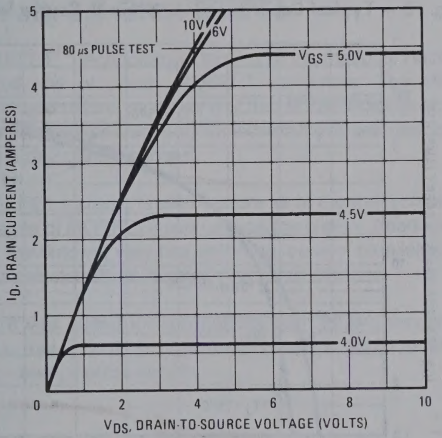


Fig. 5 — Typical Saturation Characteristics (IRF330, IRF331)

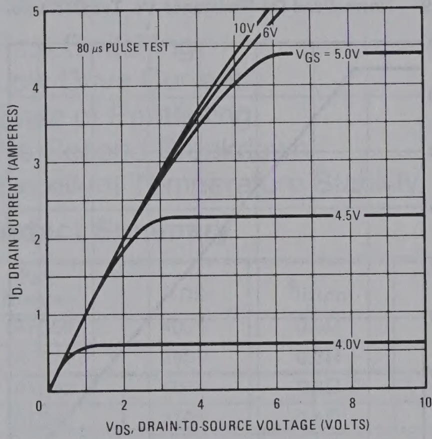


Fig. 6 — Typical Saturation Characteristics (IRF332, IRF333)

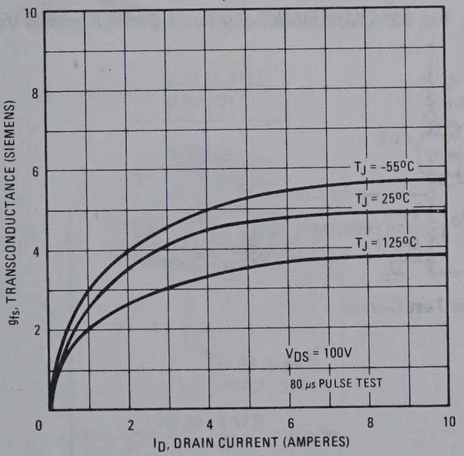


Fig 7. — Typical Transconductance Vs. Drain Current

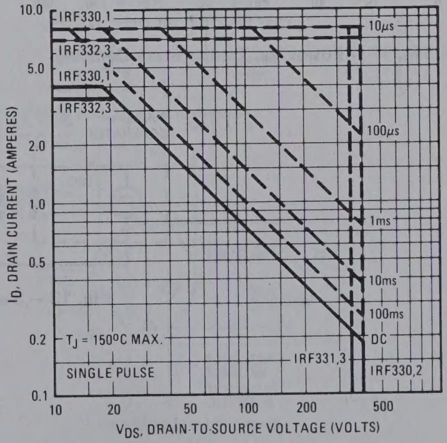


Fig. 8 — Maximum Safe Operating Area

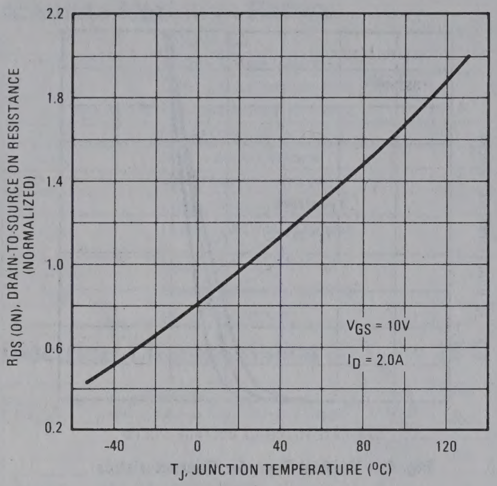


Fig. 9 — Normalized On-Resistance Vs. Temperature

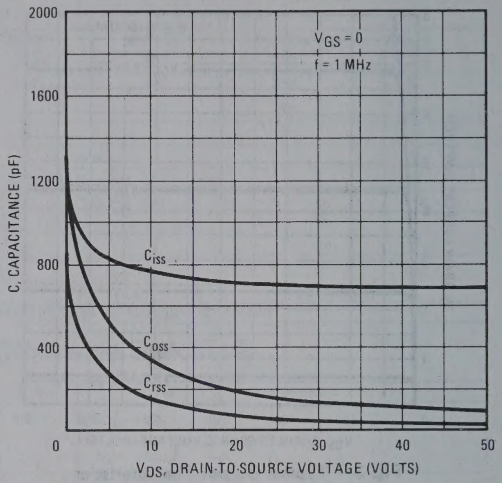


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

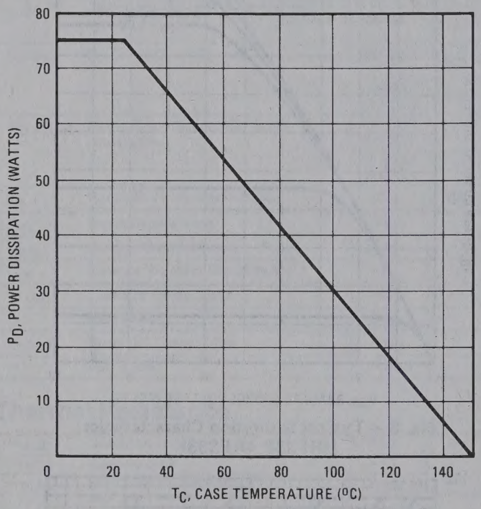


Fig. 11 — Power Vs. Temperature Derating

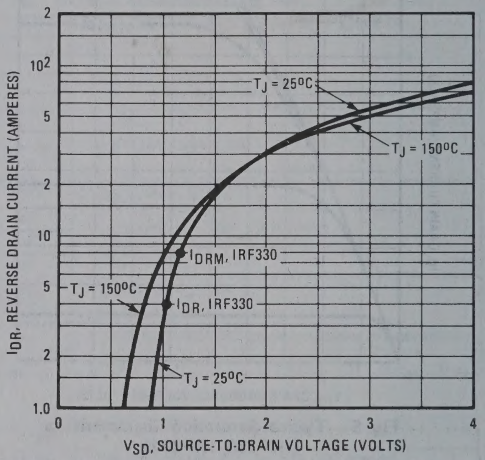


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

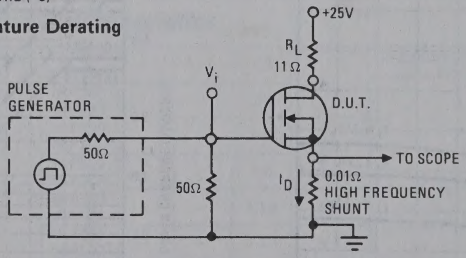
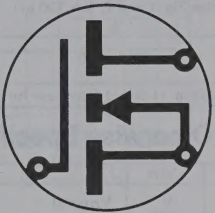


Fig. 13 — Switching Time Test Circuit

INTERNATIONAL RECTIFIER **IOR**

MOSFET TRANSISTORS

IRF350
IRF351
IRF352
IRF353



N Channel

400 Volt, 0.3 Ohm HEXFET™

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

Features:

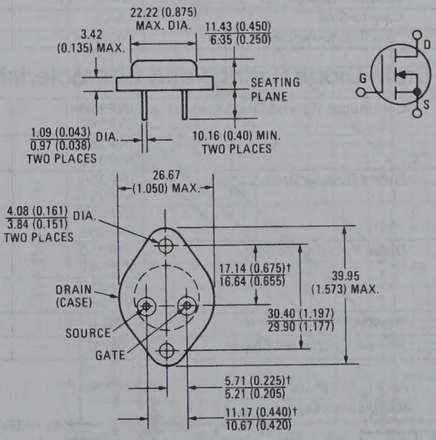
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{D(on)}$	I_D
IRF350	400V	0.3Ω	11A
IRF351	350V	0.3Ω	11A
IRF352	400V	0.4Ω	10A
IRF353	350V	0.4Ω	10A

CASE STYLE AND DIMENSIONS

ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)

Dimensions in Millimeters and (Inches)

IRF350, IRF351, IRF352, IRF353 Devices

Absolute Maximum Ratings

Parameter		IRF350	IRF351	IRF352	IRF353	Units
V_{DS}	Drain — Source Voltage	400	350	400	350	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	400	350	400	350	V
I_D @ $T_C \cong 94.0^oC$	Continuous Drain Current	11		10		A
I_{DM}	Pulsed Drain Current	25		20		A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	150 (See Fig. 11)				W
	Linear Derating Factor	1.2 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 25		20		A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10 sec)				°C

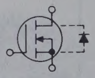
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF350 IRF352	400	—	—	V	V_{GS} = 0
		IRF351 IRF353	350	—	—	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	0.1	1.0	mA	V_{DS} = Max. Rating, V_{GS} = 0
			—	0.2	4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_J = 125°C
I_D (on)	On-State Drain Current	IRF350 IRF351	15	—	—	A	V_{DS} = 25V, V_{GS} = 10V
		IRF352 IRF353	13	—	—	A	
R_{DS} (on)	Static Drain-Source On State	IRF350 IRF351	—	0.25	0.3	Ω	V_{GS} = 10V, I_D = 5.5A
		IRF352 IRF353	—	0.3	0.4	Ω	
g_{fs}	Forward Transconductance	ALL	5.0	9.0	—	S (℧)	V_{DS} = 100V, I_D = 5.5A
C_{iss}	Input Capacitance	ALL	—	3000	4000	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	—	400	600	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	200	pF	
t_d (on)	Turn-On Delay Time	ALL	—	40	60	ns	I_D = 5.5A, E_1 = 0.5 BV_{DSS} (See Fig. 13) T_J = 125°C (MOSFET Switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	100	150	ns	
t_d (off)	Turn-Off Delay Time	ALL	—	300	400	ns	
t_f	Fall Time	ALL	—	100	150	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	0.83	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	0.2	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF350 IRF351	—	—	11	A	Modified MOSFET sybol showing the integral reverse P-N junction rectifier. 
		IRF352 IRF353	—	—	10		
I_{DRM}	Pulsed Reverse Drain Current	IRF350 IRF351	—	—	25	A	
		IRF352 IRF353	—	—	20		
V_{SD}	Diode Forward Voltage	IRF350 IRF351	—	—	1.20	V	T_J = 25°C, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF352 IRF353	—	—	1.12	V	
t_{rr}	Reverse Recovery Time	ALL	—	1000	—	ns	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	25.0	—	μC	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

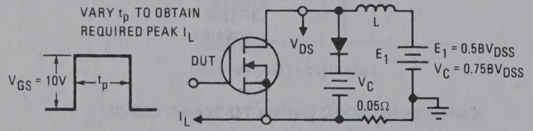


Fig. 1 — Clamped Inductive Test Circuit

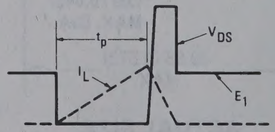


Fig. 2 — Clamped Inductive Waveforms

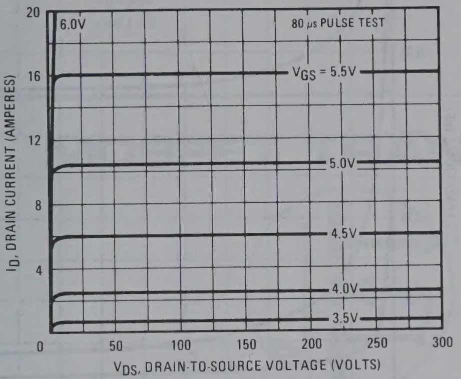


Fig. 3 – Typical Output Characteristics

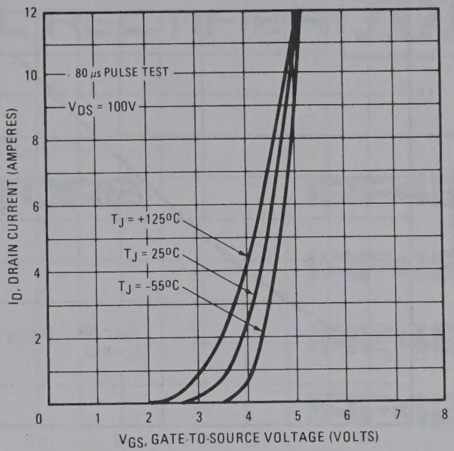


Fig. 4 – Typical Transfer Characteristics

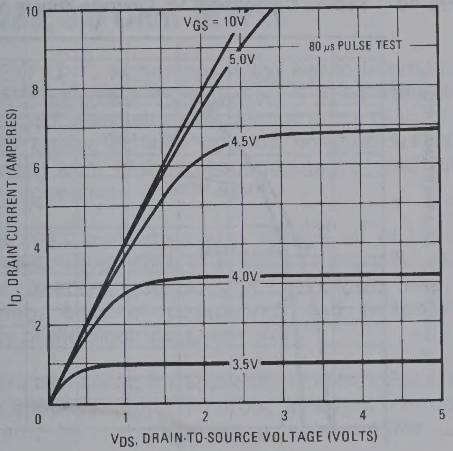


Fig. 5 – Typical Saturation Characteristics (IRF350, IRF351)

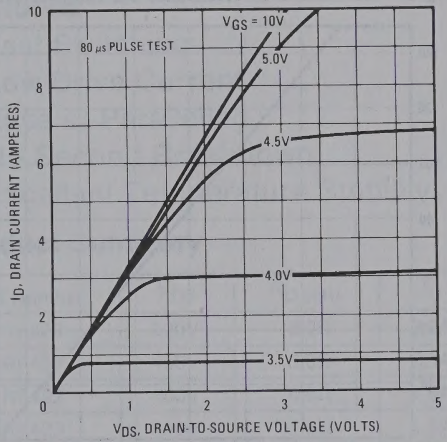


Fig. 6 – Typical Saturation Characteristics (IRF352, IRF353)

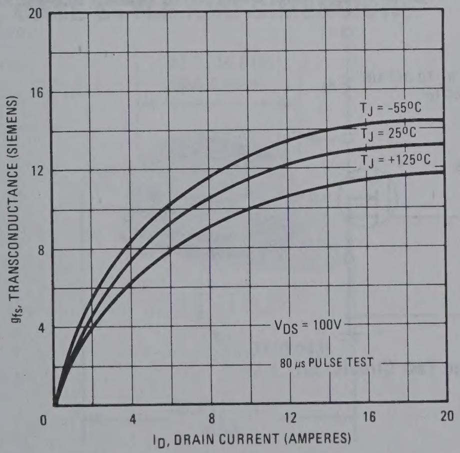


Fig. 7 – Typical Transconductance Vs. Drain Current

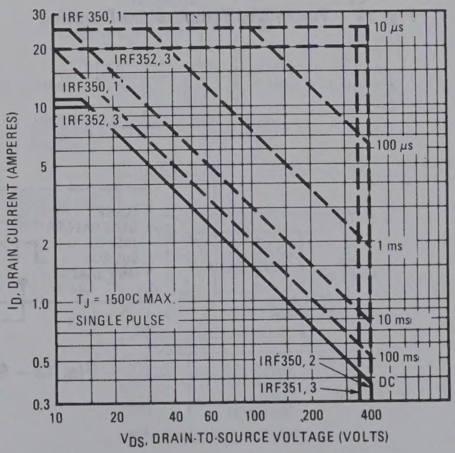


Fig. 8 – Maximum Safe Operating Area

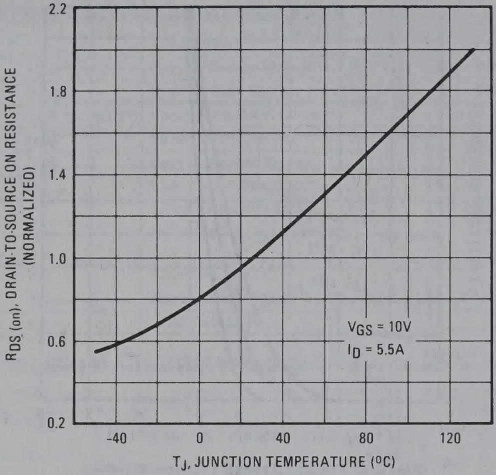


Fig. 9 — Normalized On-Resistance Vs. Temperature

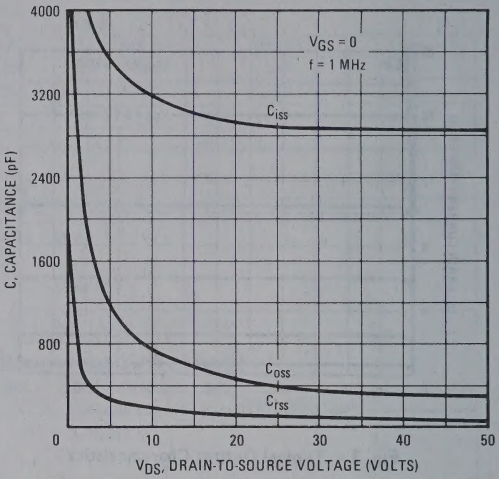


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

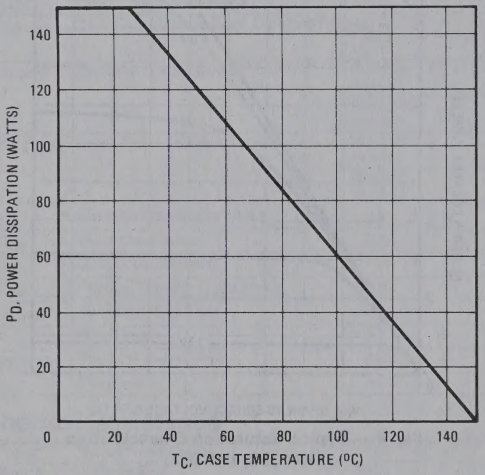


Fig. 11 — Power Vs. Temperature Derating

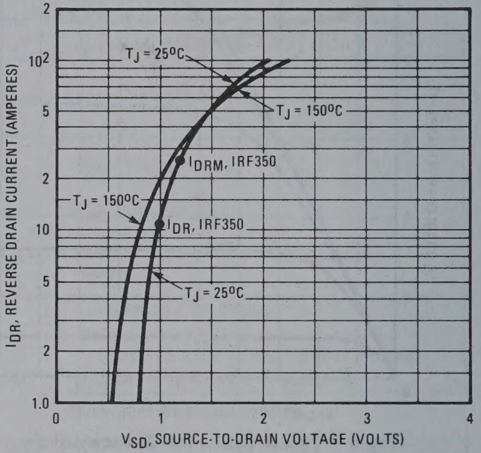


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

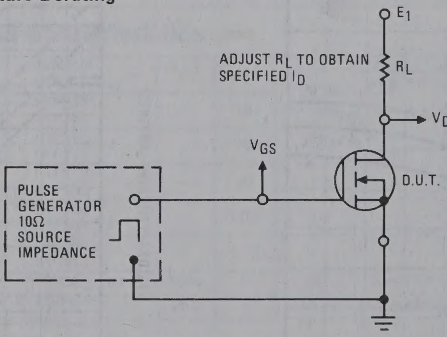
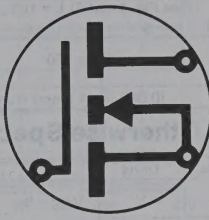

E_1
ADJUST R_L TO OBTAIN SPECIFIED I_D
R_L
V_DS
V_GS
D.U.T.
PULSE GENERATOR 10Ω SOURCE IMPEDANCE

Fig. 13 — Switching Time Test Circuit

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS

IRF420
IRF421
IRF422
IRF423



N Channel

500 Volt, 3.0 Ohm HEXFET™

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

Features:

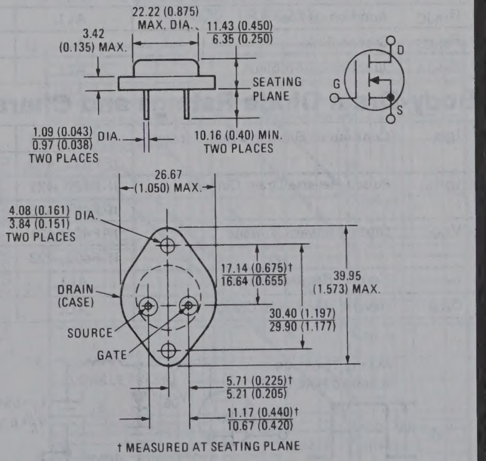
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{D\,(on)}$	I_D
IRF420	500V	3.0Ω	2.0A
IRF421	450V	3.0Ω	2.0A
IRF422	500V	4.0Ω	1.5A
IRF423	450V	4.0Ω	1.5A

CASE STYLE AND DIMENSIONS

ACTUAL SIZE



Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Inches and (Millimeters)

Absolute Maximum Ratings

Parameter		IRF420	IRF421	IRF422	IRF423	Units
V_{DS}	Drain — Source Voltage	500	450	500	450	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	500	450	500	450	V
I_D @ $T_C \cong 89.5^oC$	Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM}	Pulsed Drain Current	5	5	4	4	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	40 (See Fig. 11)				W
	Linear Derating Factor	0.32 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH				A
		5	5	4	4	
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC
	Lead Temperature	300	(0.063 in. (1.6mm) from case for 10s)			^oC

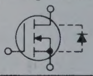
Electrical Characteristics @ $T_C = 25°C$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF420 IRF422	500	—	—	V	V_{GS} = 0
		IRF421 IRF423	450	—	—	V	I_D = 4.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	0.1	1.0	mA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0
			—	0.2	4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_J = 25°C to 125°C
$I_{D\ (on)}$	On-State Drain Current	IRF420 IRF421	2.5	—	—	A	V_{DS} = 25V, V_{GS} = 10V
		IRF422 IRF423	2.0	—	—	A	
$R_{DS\ (on)}$	Static Drain-Source On State Resistance	IRF420 IRF421	—	2.5	3.0	Ω	V_{GS} = 10V, I_D = 1A
		IRF422 IRF423	—	3.0	4.0	Ω	
g_{fs}	Forward Transconductance	ALL	1.0	1.75	—	S (℧)	V_{DS} = 100V, I_D = 1A
C_{iss}	Input Capacitance	ALL	—	300	400	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	—	75	150	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	40	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	—	30	60	ns	I_D = 1A, E_1 = 0.5 BV_{DSS}
t_r	Rise Time	ALL	—	25	50	ns	(See Fig. 13)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	—	30	60	ns	T_J = 125°C (MOSFET Switching times are essen-
t_f	Fall Time	ALL	—	15	30	ns	tially independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	0.2	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF420, 421	—	—	2.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF422, 423	—	—	1.5		
I_{DRM}	Pulsed Reverse Drain Current	IRF420, 421	—	—	5.0	A	
		IRF422, 423	—	—	4.0		
V_{SD}	Diode Forward Voltage	IRF420, 421	—	—	1.0	V	T_J = 25°C, I_F = I_{DRM}, V_{GS} = 0V
		IRF422, 423	—	—	0.9		
t_{rr}	Reverse Recovery Time	ALL	—	200	—	ns	T_J = 150°C, I_F = I_{DRM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	3.0	—	μC	T_J = 150°C, I_F = I_{DRM}, dI_F/dt = 100 A/μs

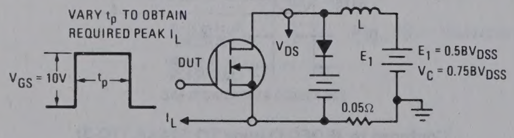


Fig. 1 — Clamped Inductive Test Circuit

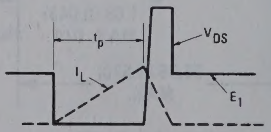


Fig. 2 — Clamped Inductive Waveforms

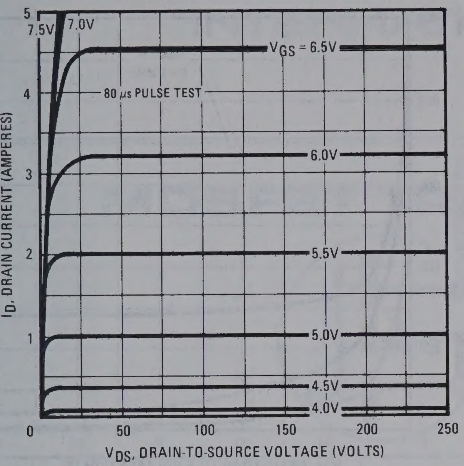


Fig. 3 – Typical Output Characteristics

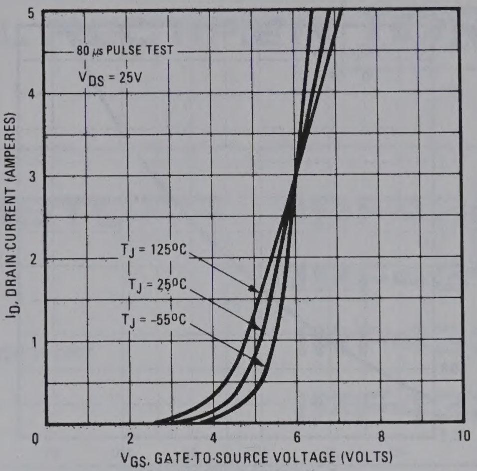


Fig. 4 – Typical Transfer Characteristics

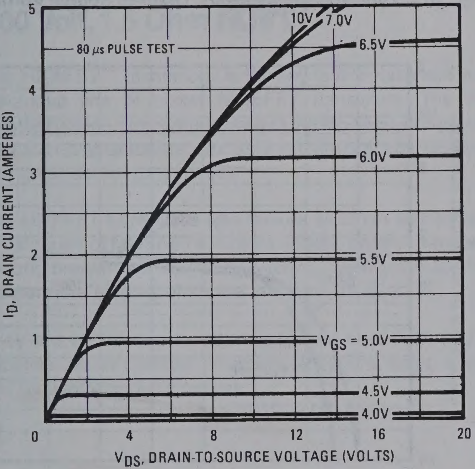


Fig. 5 – Typical Saturation Characteristics (IRF420, IRF421)

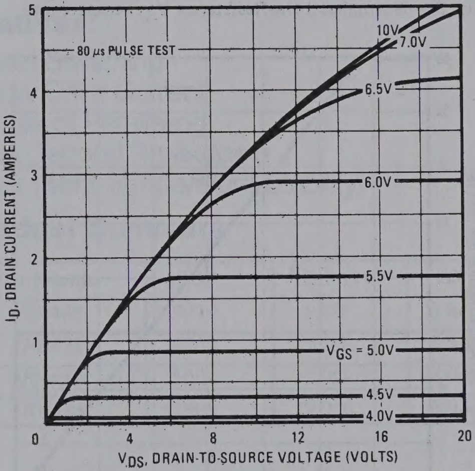


Fig. 6 – Typical Saturation Characteristics (IRF422, IRF423)

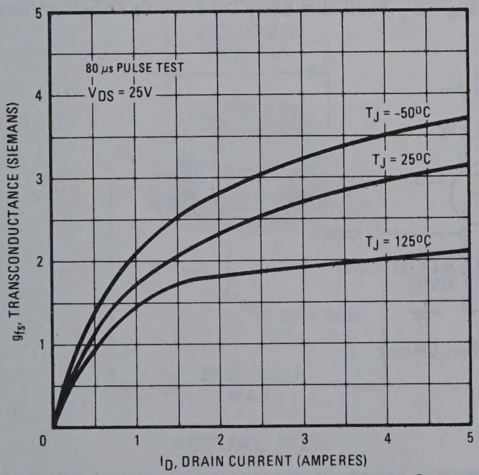


Fig. 7 – Typical Transconductance Vs. Drain Current

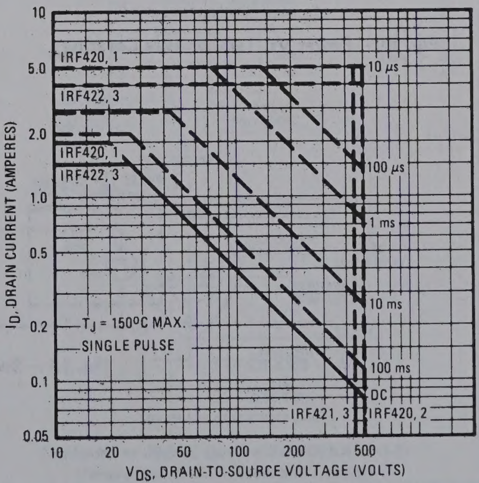


Fig. 8 – Maximum Safe Operating Area

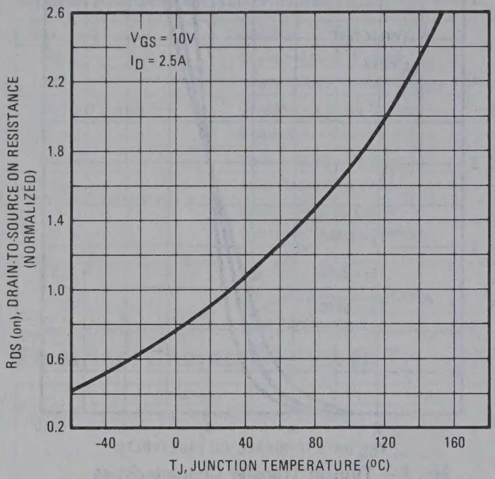


Fig. 9 – Normalized On-Resistance Vs. Temperature

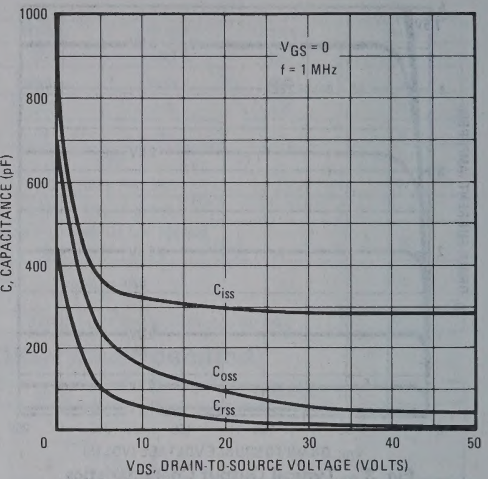


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

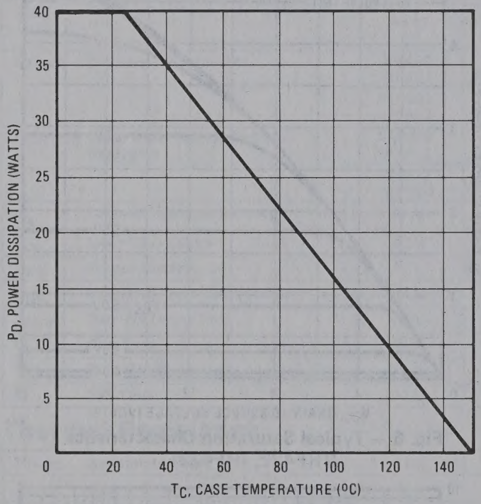


Fig. 11 – Power Vs. Temperature Derating

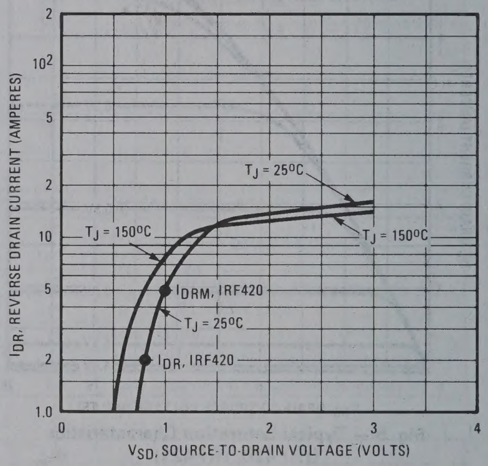


Fig. 12 – Maximum Body-Drain Diode Forward Voltage

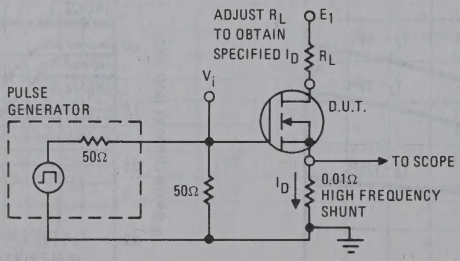
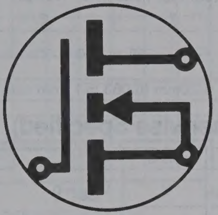

ADJUST R_L TO OBTAIN SPECIFIED I_D
E_1
R_L
V_i
PULSE GENERATOR
50Ω
D.U.T.
TO SCOPE
50Ω
I_D
0.01Ω HIGH FREQUENCY SHUNT

Fig. 13 – Switching Time Test Circuit

PD-9.310

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF430 IRF431 IRF432 IRF433



N Channel

500 Volt, 1.5 Ohm HEXFET™

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

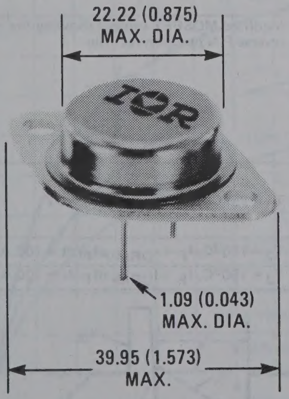
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

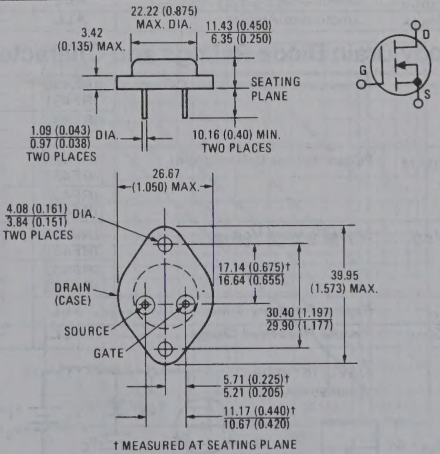
Product Summary

Part Number	V_{DS}	R_D (on)	I_D
IRF430	500V	1.5Ω	3.5A
IRF431	450V	1.5Ω	3.5A
IRF432	500V	2.0Ω	3.0A
IRF433	450V	2.0Ω	3.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

IRF430, IRF431, IRF432, IRF433 Devices

Absolute Maximum Ratings

Parameter		IRF430	IRF431	IRF432	IRF433	Units
V_{DS}	Drain — Source Voltage	500	450	500	450	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	500	450	500	450	V
I_D @ $T_C \cong 91.0^oC$	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current	7.0	7.0	6.0	6.0	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	75 (See Fig. 11)				W
	Linear Derating Factor	0.6 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH				A
		7	7	6	6	
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC
	Lead Temperature	300 (1.6mm (0.063 in.) from case for 10s)				^oC

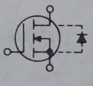
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF430 IRF432	500	—	—	V	$V_{GS} = 0$
		IRF431 IRF433	450	—	—	V	I_D = 4.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	0.1	1.0	mA	V_{DS} = 0.8 x Max. Rating, $V_{GS} = 0$
			—	0.2	4.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_J = 25^oC$ to 125^oC
I_D (on)	On-State Drain Current	IRF430 IRF431	5.0	—	—	A	V_{DS} = 25V, V_{GS} = 10V
		IRF432 IRF433	4.0	—	—	A	
R_{DS} (on)	Static Drain-Source On State Resistance	IRF430 IRF431	—	1.3	1.5	Ω	V_{GS} = 10V, I_D = 1.5A
		IRF432 IRF433	—	1.5	2.0	Ω	
g_{fs}	Forward Transconductance	ALL	1.5	2.5	—	S (℧)	V_{DS} = 100V, I_D = 1.5A
C_{iss}	Input Capacitance	ALL	—	700	900	pF	$V_{GS} = 0$, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	—	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	30	60	pF	
t_d (on)	Turn-On Delay Time	ALL	—	30	50	ns	I_D = 1.5A, $E_1 = 0.5\ BV_{DSS}$ (See Fig. 13) $T_J = 125^oC$ (MOSFET Switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	40	80	ns	
t_d (off)	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	40	80	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	0.2	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF430 IRF431	—	—	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF432 IRF433	—	—	3.0		
I_{DRM}	Pulsed Reverse Drain Current	IRF430 IRF431	—	—	7.0	A	
		IRF432 IRF433	—	—	6.0		
V_{SD}	Diode Forward Voltage	IRF430 IRF431	—	—	1.13	V	$T_J = 25^oC$, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF432 IRF433	—	—	1.10	V	
t_{rr}	Reverse Recovery Time	ALL	—	500	—	ns	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	7.0	—	μC	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

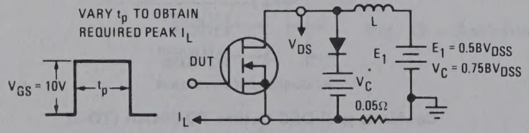


Fig. 1 — Clamped Inductive Test Circuit

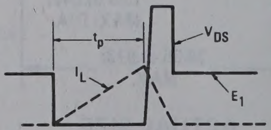


Fig. 2 — Clamped Inductive Waveforms

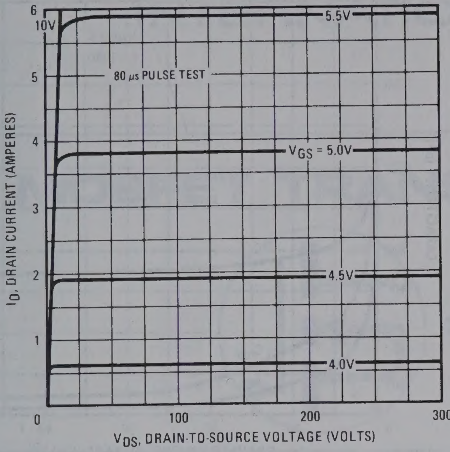


Fig. 3 — Typical Output Characteristics

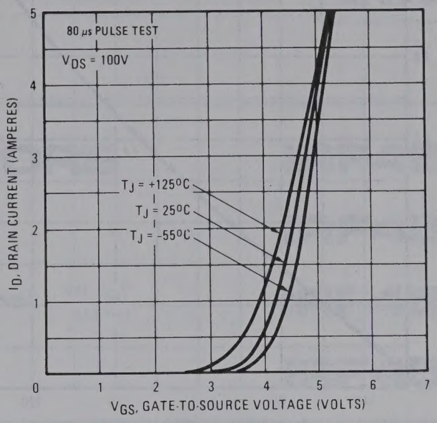


Fig. 4 — Typical Transfer Characteristics

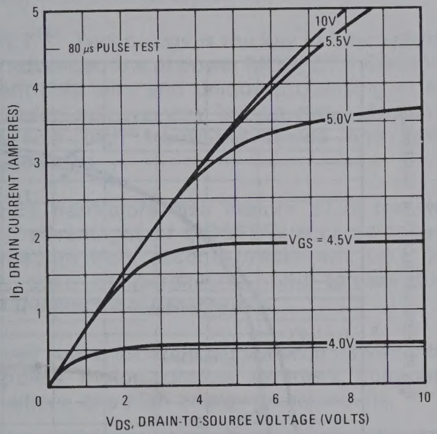


Fig. 5 — Typical Saturation Characteristics
(IRF430, IRF431)

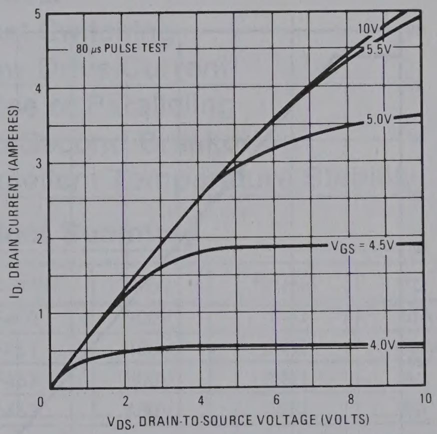


Fig. 6 — Typical Saturation Characteristics
(IRF432, IRF433)

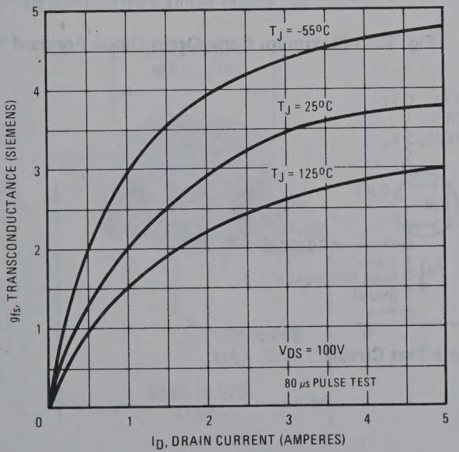


Fig. 7 — Typical Transconductance Vs. Drain Current

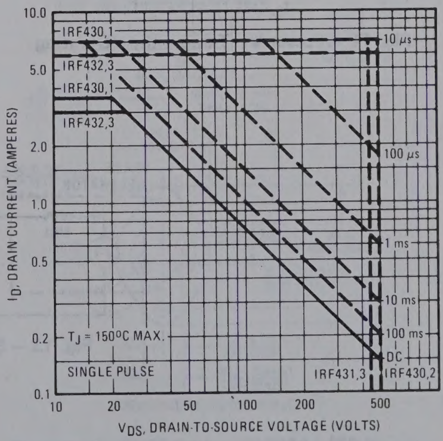


Fig. 8 — Maximum Safe Operating Area

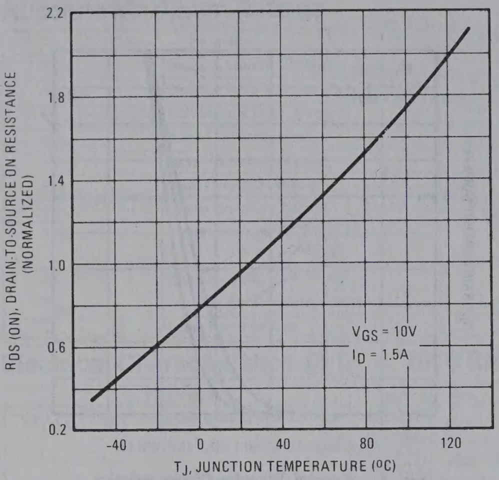


Fig. 9 – Normalized On-Resistance Vs. Temperature

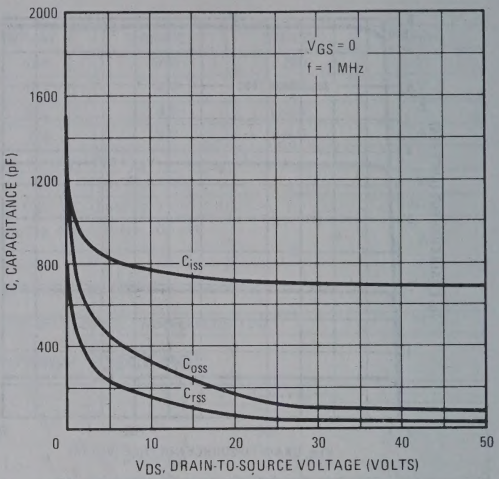


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

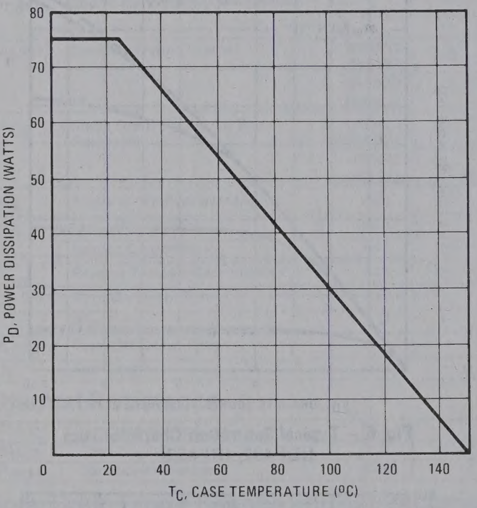


Fig. 11 – Power Vs. Temperature Derating

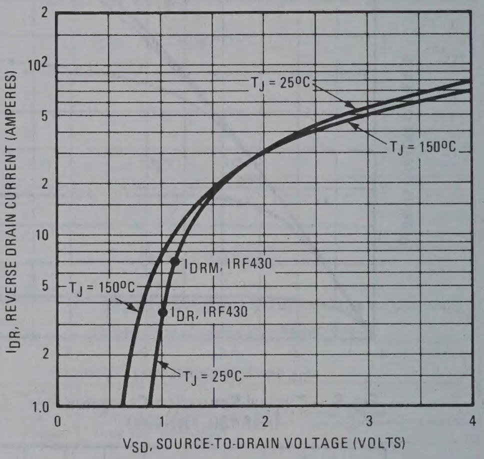


Fig. 12 – Maximum Body-Drain Diode Forward Voltage

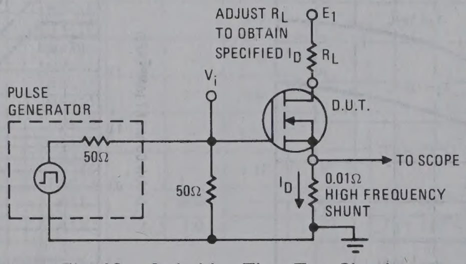
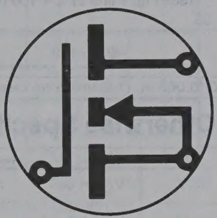


Fig. 13 – Switching Time Test Circuit

INTERNATIONAL RECTIFIER **IOR**

MOSFET TRANSISTORS

IRF450
IRF451
IRF452
IRF453



N Channel

500 Volt, 0.4 Ohm HEXFET™

The HEXFET™ Technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

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They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

Features:

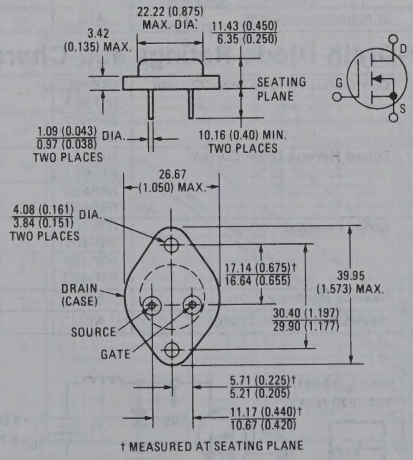
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{D(on)}$	I_D
IRF450	500V	0.4Ω	10A
IRF451	450V	0.4Ω	10A
IRF452	500V	0.5Ω	8A
IRF453	450V	0.5Ω	8A

CASE STYLE AND DIMENSIONS

ACTUAL SIZE



Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings

	Parameter	IRF450	IRF451	IRF452	IRF453	Units
V_{DS}	Drain – Source Voltage	500	450	500	450	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	500	450	500	450	V
I_D @ $T_C \cong 90^oC$	Continuous Drain Current	10		8		A
I_{DM}	Pulsed Drain Current	25		20		A
V_{GS}	Gate – Source Voltage	±20				V
P_D	Max. Power Dissipation	150 (See Fig. 11)				W
	Linear Derating Factor	1.2 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 25		20		A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				^oC

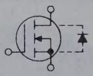
Electrical Characteristics @ T_C =25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRF450 IRF452	500	–	–	V	V_{GS} = 0
		IRF451 IRF453	450	–	–	V	I_D = 4.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate – Body Leakage	ALL	–	–	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0	mA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0
			–	0.2	4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_J = 25°C to 125°C
I_D (on)	On-State Drain Current	IRF450 IRF451	13	–	–	A	V_{DS} = 25V, V_{GS} = 10V
		IRF452 IRF453	12	–	–	A	
R_{DS} (on)	Static Drain-Source On State	IRF450 IRF451	–	0.3	0.4	Ω	V_{GS} = 10V, I_D = 5A
		IRF452 IRF453	–	0.4	0.5	Ω	
g_{fs}	Forward Transconductance	ALL	6	10	–	S (℧)	V_{DS} = 25V, I_D = 5A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	–	400	600	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	200	pF	
t_d (on)	Turn-On Delay Time	ALL	–	40	60	ns	I_D = 5A, E_1 = 0.5 BV_{DSS} See Fig. 13 T_J = 125°C (MOSFET Switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	60	100	ns	
t_d (off)	Turn-Off Delay Time	ALL	–	200	300	ns	
t_f	Fall Time	ALL	–	90	140	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83	K/W	
R_{thCS}	Case-to-Sink	ALL	–	–	0.2	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF450 IRF451	–	–	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF452 IRF453	–	–	8		
I_{DRM}	Pulsed Reverse Drain Current	IRF450 IRF451	–	–	25	A	
		IRF452 IRF453	–	–	20		
V_{SD}	Diode Forward Voltage	IRF450 IRF451	–	–	1.13	V	T_J = 25°C, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF452 IRF453	–	–	1.10	V	
t_{rr}	Reverse Recovery Time	ALL	–	400	–	ns	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

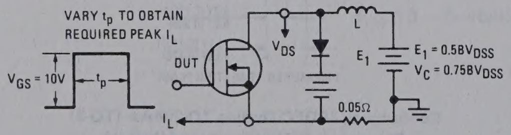


Fig. 1 – Clamped Inductive Test Circuit

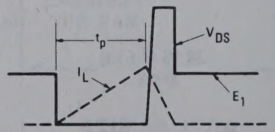


Fig. 2 – Clamped Inductive Waveforms

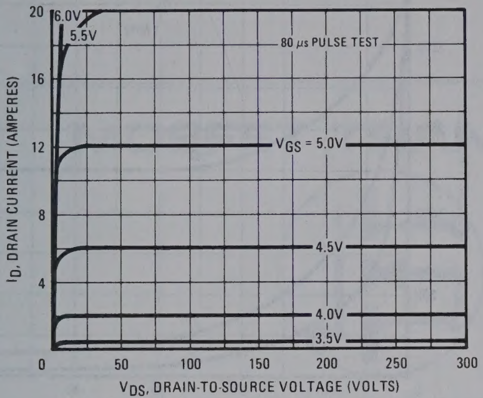


Fig. 3 – Typical Output Characteristics

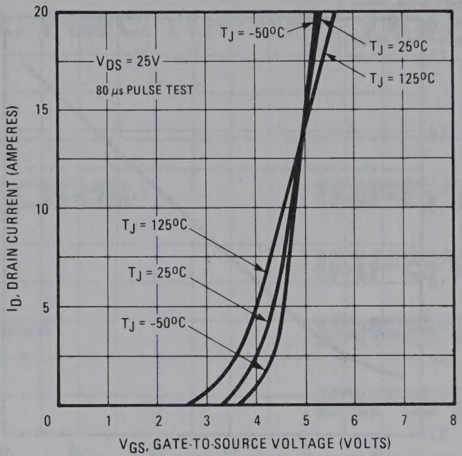


Fig. 4 – Typical Transfer Characteristics

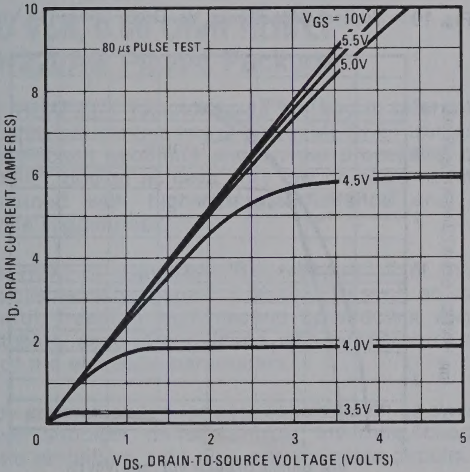


Fig. 5 – Typical Saturation Characteristics (IRF450, IRF451)

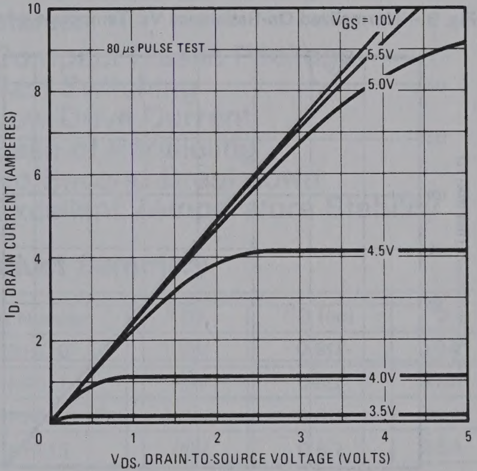


Fig. 6 – Typical Saturation Characteristics (IRF452, IRF453)

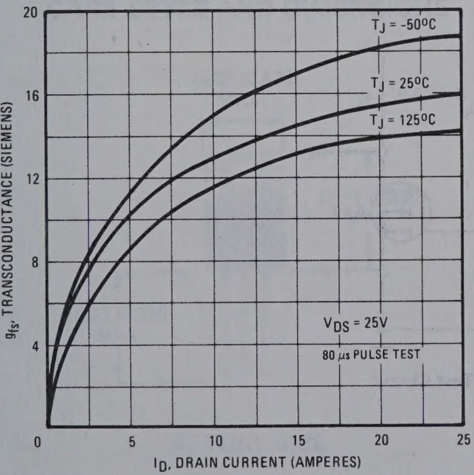


Fig. 7 – Typical Transconductance Vs. Drain Current

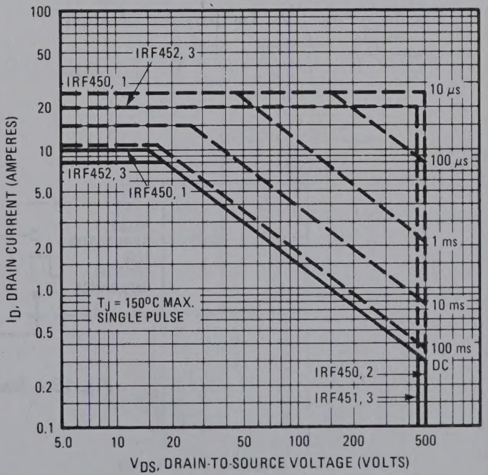


Fig. 8 – Maximum Safe Operating Area

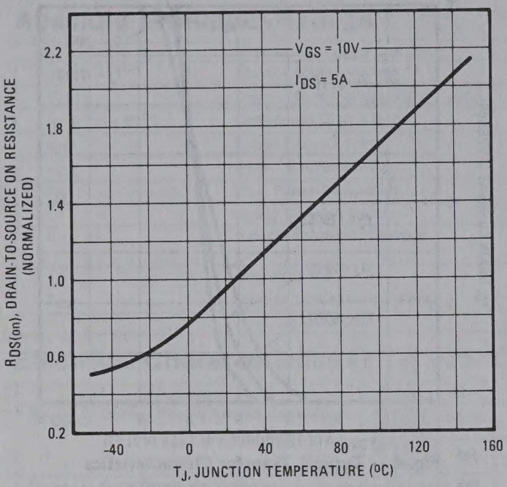


Fig. 9 – Normalized On-Resistance Vs. Temperature

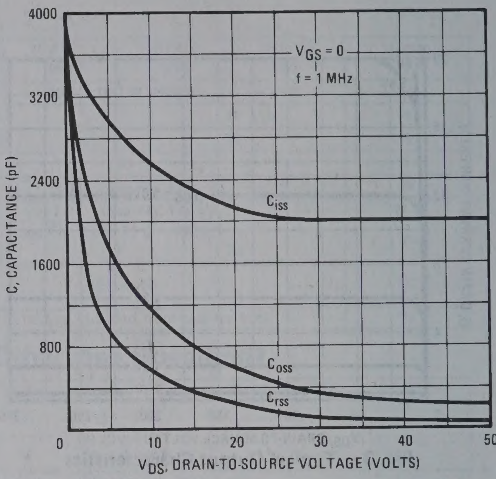


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

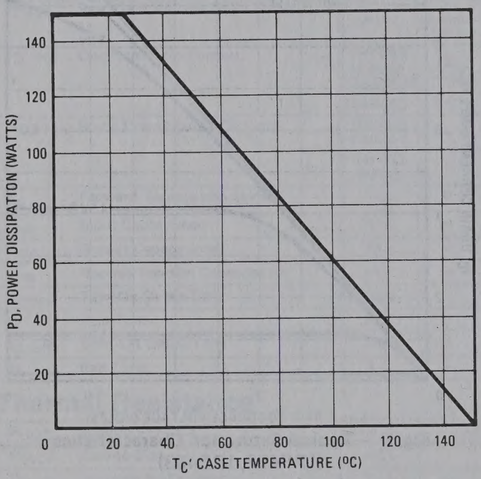


Fig. 11 – Power Vs. Temperature Derating

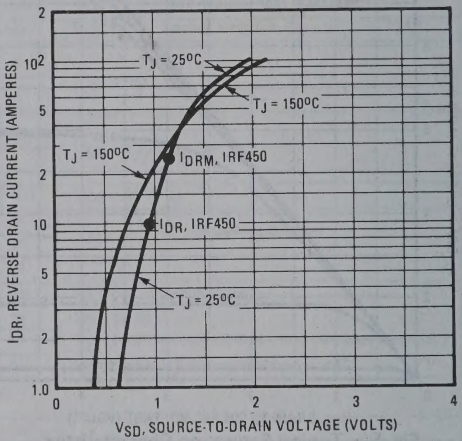


Fig. 12 – Maximum Body-Drain Diode Forward Voltage

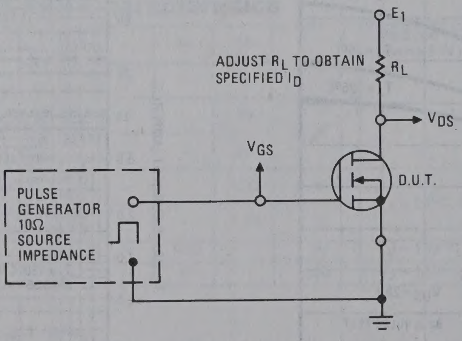

E_1
ADJUST R_L TO OBTAIN SPECIFIED I_D
R_L
V_{DS}
V_{GS}
D.U.T.
PULSE GENERATOR 10Ω SOURCE IMPEDANCE

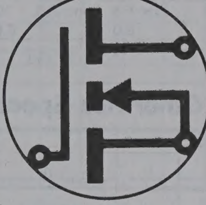
Fig. 13 – Switching Time Test Circuit

PD-9.325

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS

IRF510
IRF511
IRF512
IRF513



100 Volt, 0.60 Ohm HEXFET™ TO-220AB Plastic Package

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

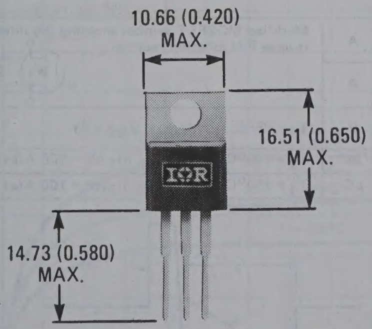
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

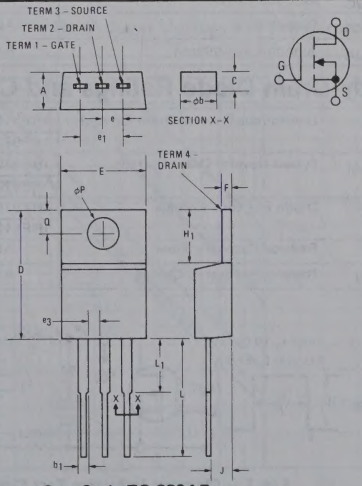
Product Summary

Part Number	V_{DS}	R_D (on)	I_D
IRF510	100V	0.6Ω	3.0A
IRF511	60V	0.6Ω	3.0A
IRF512	100V	0.8Ω	2.5A
IRF513	60V	0.8Ω	2.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB

Refer to page 158 for Case Style Dimension Table.

Absolute Maximum Ratings

	Parameter	IRF510	IRF511	IRF512	IRF513	Units
V_{DS}	Drain – Source Voltage	100	60	100	60	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	100	60	100	60	V
I_D @ $T_C \cong 86^oC$	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current	8.0	8.0	6.0	6.0	A
V_{GS}	Gate – Source Voltage	±20				V
P_D	Max. Power Dissipation	20 (See Fig. 11)				W
	Linear Derating Factor	0.16 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 µH 8.0	8.0	6.0	6.0	A
T_J T_{stg}	Operating and Storage Temperature Range	−55 to 150				^oC

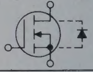
Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRF510 IRF512	100	–	–	V	V_{GS} = 0
		IRF511 IRF513	60	–	–	V	I_D = 0.5 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 0.5 mA
I_{GSS}	Gate – Body Leakage	ALL	–	–	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	0.5	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	2.0	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_J = 125°C
$I_{D\ (on)}$	On-State Drain Current	IRF510 IRF511	4.0	–	–	A	V_{DS} = 25V, V_{GS} = 10V
		IRF512 IRF513	3.5	–	–	A	
$R_{DS\ (on)}$	Static Drain-Source On-State Resistance	IRF510 IRF511	–	0.5	0.6	Ω	V_{GS} = 10V, I_D = 1.5A
		IRF512 IRF513	–	0.6	0.8	Ω	
g_{fs}	Forward Transconductance	ALL	1.0	1.5	–	S (℧)	V_{DS} = 25V, I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	135	150	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	80	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	25	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	10	20	ns	I_D = 1.5, E_1 = 0.5 BV_{DSS}, V_{GS} = 10V (See Fig. 13) T_J = 125°C (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	6.4	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.5	–	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF510, 511	–	–	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF512, 513	–	–	2.5		
I_{DRM}	Pulsed Reverse Drain Current	IRF510, 511	–	–	8.0	A	
		IRF512, 513	–	–	6.0		
V_{SD}	Diode Forward Voltage	IRF510, 511	–	–	2.9	V	T_J = 25°C, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF512, 513	–	–	1.9		
t_{rr}	Reverse Recovery Time	ALL	–	100	–	ns	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/µs
Q_{RR}	Reverse Recovered Charge	ALL	–	0.2	–	µC	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/µs

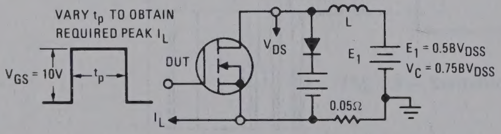


Fig. 1 — Clamped Inductive Test Circuit

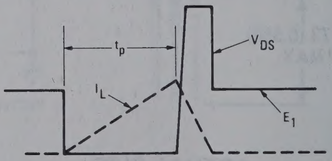


Fig. 2 — Clamped Inductive Waveforms

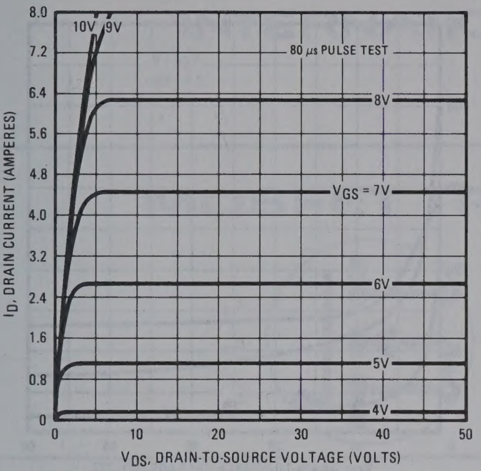


Fig. 3 — Typical Output Characteristics

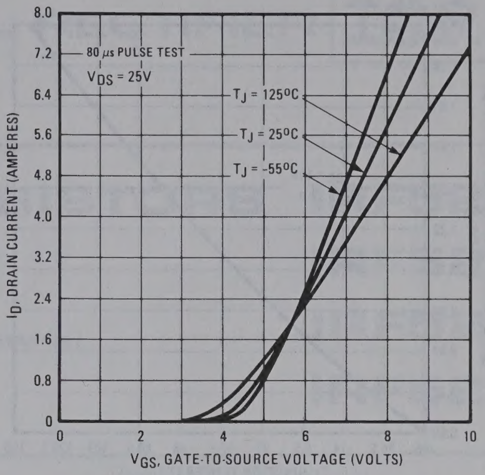


Fig. 4 — Typical Transfer Characteristics

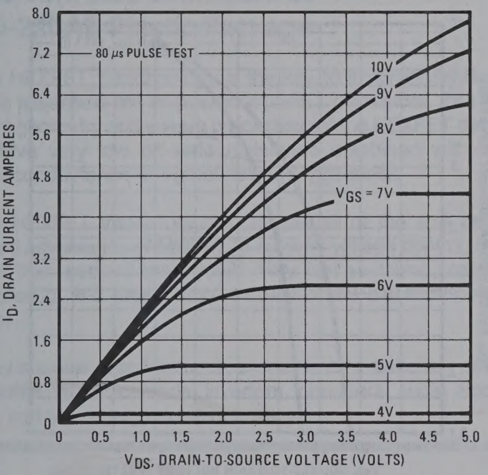


Fig. 5 — Typical Saturation Characteristics

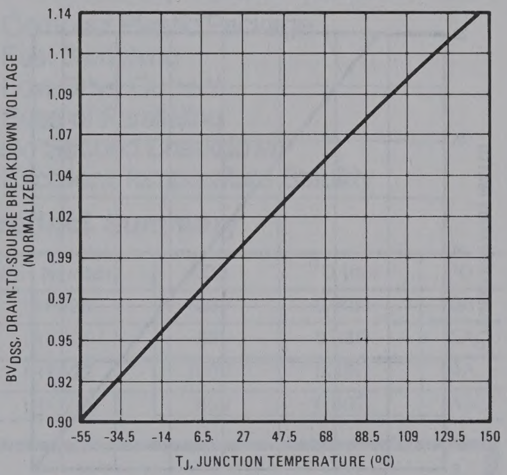


Fig. 6 — Breakdown Voltage Vs. Temperature

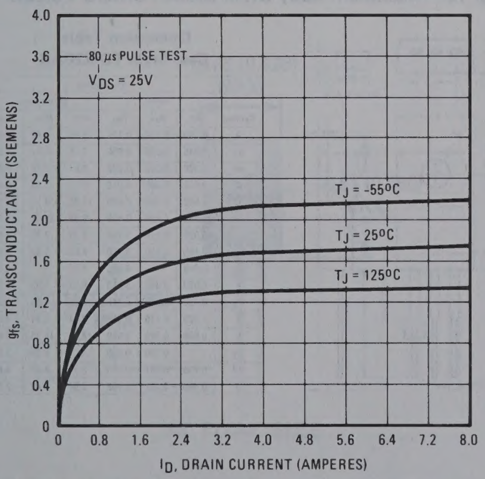


Fig. 7 — Typical Transconductance Vs. Drain Current

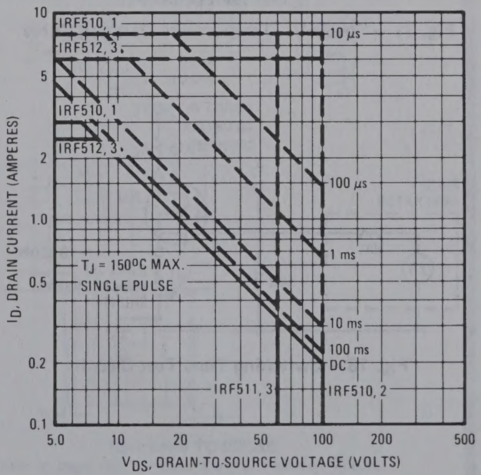


Fig. 8 — Maximum Safe Operating Area

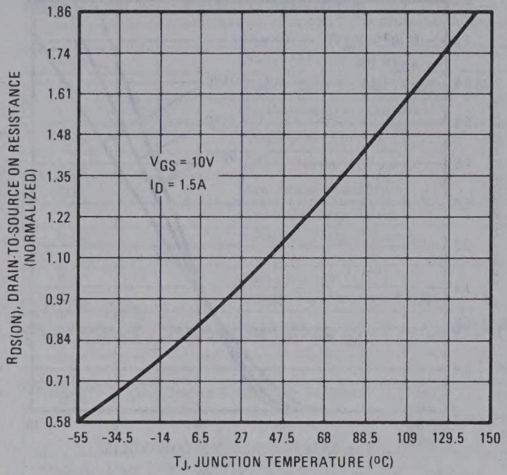


Fig. 9 — Normalized On-Resistance Vs. Temperature

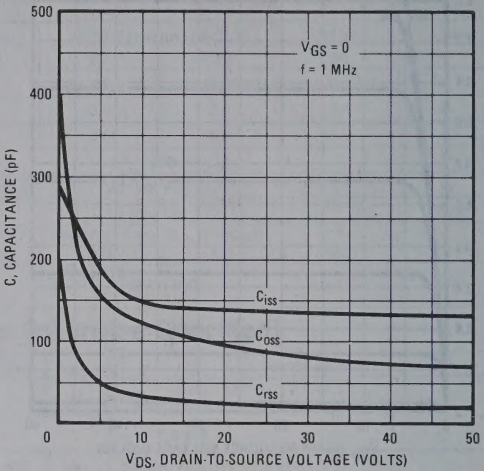


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

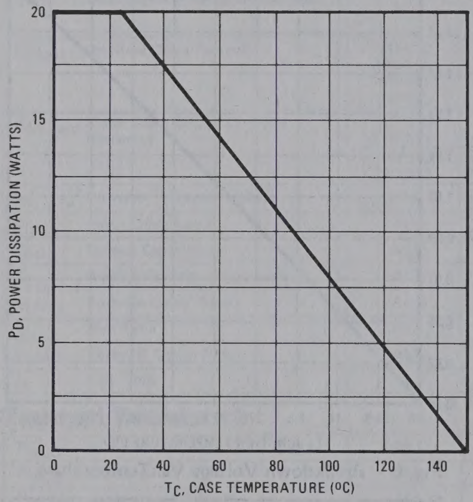


Fig. 11 — Power Vs. Temperature Derating Curve

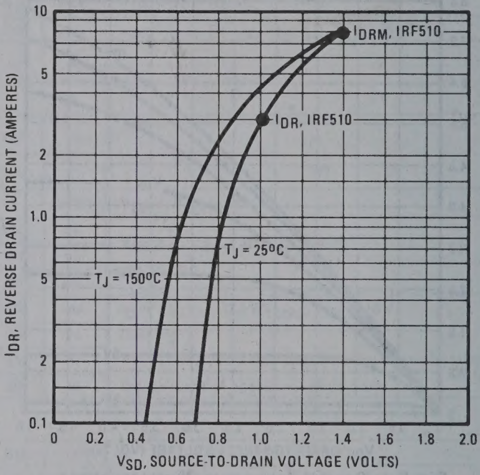


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

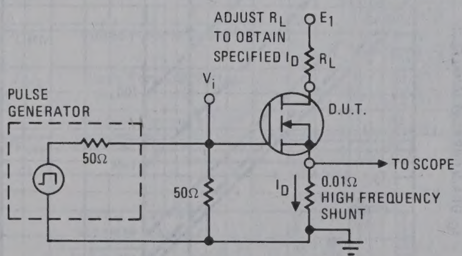
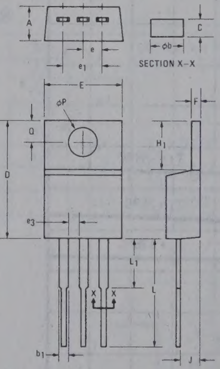

ADJUST R_L TO OBTAIN SPECIFIED I_D
E_1
R_L
V_i
PULSE GENERATOR
50Ω
50Ω
D.U.T.
TO SCOPE
I_D
0.01Ω HIGH FREQUENCY SHUNT

Fig. 13 — Switching Time Test Circuit

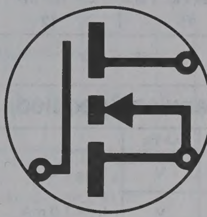


Dimension Table, Case Style TO-220AB

	Dimensions					
	Inches			Millimeters		
Symbol	Min.	Max.	Typ.	Min.	Max.	Typ.
A	0.140	0.190	0.175	3.56	4.82	4.45
b_1	0.045	0.070	0.050	1.15	1.77	1.27
ϕb	0.020	0.045	0.032	0.51	1.14	0.81
C	0.012	0.045	0.018	0.31	1.14	0.46
D	0.560	0.650	0.590	14.23	16.51	14.99
E	0.380	0.420	0.400	9.66	10.66	10.16
e	0.090	0.110	0.100	2.29	2.79	2.54
e_1	0.190	0.210	0.200	4.83	5.33	5.08
e_3	0.045	–	0.050	1.15	–	1.27
F	0.020	0.055	0.050	0.51	1.39	1.27
H_1	0.230	0.270	0.248	5.85	6.85	6.30
J	0.080	0.115	0.105	2.04	2.92	2.67
L	0.500	0.580	0.550	12.70	14.73	13.98
L_1	–	0.250	0.230	–	6.35	5.84
ϕP	0.139	0.161	0.145	3.54	4.08	3.68
Q	0.100	0.135	0.108	2.54	3.42	2.74

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF520 IRF521 IRF522 IRF523



N Channel

100 Volt, 0.30 Ohm HEXFET™ TO-220AB Plastic Package

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

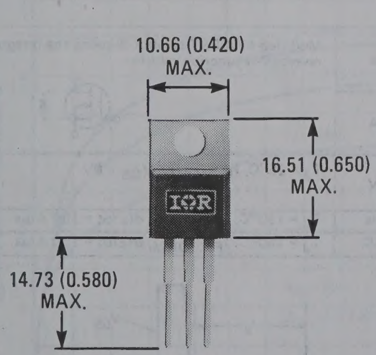
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

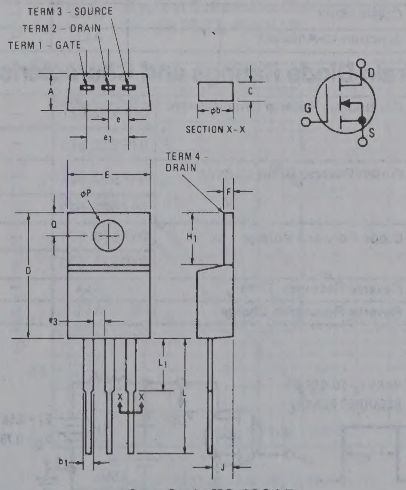
Product Summary

Part Number	V_{DS}	R_D (on)	I_D
IRF520	100V	0.30Ω	5A
IRF521	60V	0.30Ω	5A
IRF522	100V	0.40Ω	4A
IRF523	60V	0.40Ω	4A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB

Refer to page 162 for Case Style Dimension Table.

Absolute Maximum Ratings

	Parameter	IRF520	IRF521	IRF522	IRF523	Units
V_{DS}	Drain – Source Voltage	100	60	100	60	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	100	60	100	60	V
I_D @ $T_C \cong 96.5^oC$	Continuous Drain Current	5	5	4	4	A
I_{DM}	Pulsed Drain Current	15	15	12	12	A
V_{GS}	Gate – Source Voltage	±20				V
P_D	Max. Power Dissipation	40 (See Fig. 11)				W
	Linear Derating Factor	0.32 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 15	15	12	12	A
T_J T_{stg}	Operating and Storage Temperature Range	−55 to 150				^oC

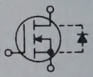
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRF520 IRF522	100	–	–	V	$V_{GS} = 0$
		IRF521 IRF523	60	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate – Body Leakage	ALL	–	–	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0$
			–	0.2	4.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_J = 125^oC$
$I_{D\ (on)}$	On-State Drain Current	IRF520 IRF521	8.0	–	–	A	V_{DS} = 25V, V_{GS} = 10V
		IRF522 IRF523	7.0	–	–	A	
$R_{DS\ (on)}$	Static Drain-Source On State Resistance	IRF520 IRF521	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 3A
		IRF522 IRF523	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance	ALL	1.5	2.5	–	S (℧)	V_{DS} = 25V, I_D = 3A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	$V_{GS} = 0$, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	100	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	20	40	ns	I_D = 3A, $E_1 = 0.5\ BV_{DSS}$ (See Fig. 13) $T_J = 125^oC$ (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	35	70	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	–	1.0	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF520, 521	–	–	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF522, 523	–	–	4.0		
I_{DRM}	Pulsed Reverse Drain Current	IRF520, 521	–	–	15	A	
		IRF522, 523	–	–	12		
V_{SD}	Diode Forward Voltage	IRF520, 521	–	–	1.90	V	$T_J = 25^oC$, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF522, 523	–	–	1.70		
t_{rr}	Reverse Recovery Time	ALL	–	150	–	ns	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.0	–	μC	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

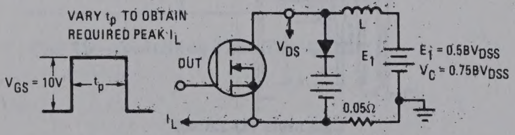

VARY t_p TO OBTAIN REQUIRED PEAK I_L
V_{GS} = 10V
t_p
OUT
V_{DS}
L
E_1
$E_1 = 0.5BV_{DSS}$
$V_C \approx 0.75BV_{DSS}$
0.05Ω
I_L

Fig. 1 – Clamped Inductive Test Circuit

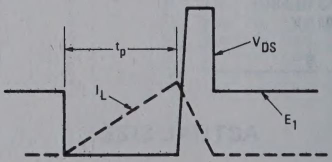


Fig. 2 – Clamped Inductive Waveforms

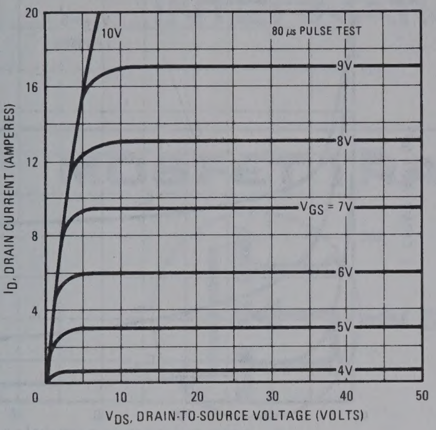


Fig. 3 – Typical Output Characteristics

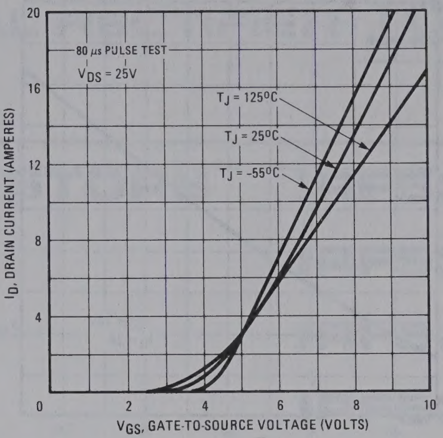


Fig. 4 – Typical Transfer Characteristics

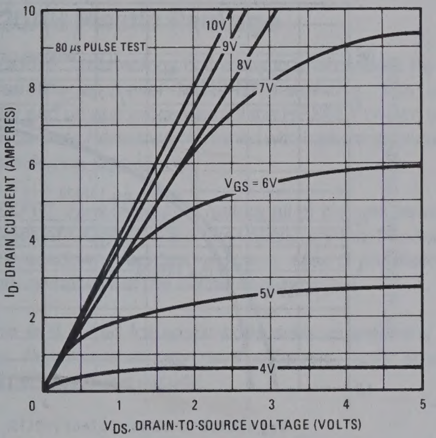


Fig. 5 – Typical Saturation Characteristics (IRF520, IRF521)

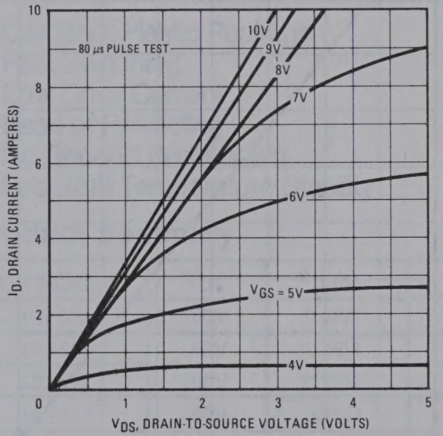


Fig. 6 – Typical Saturation Characteristics (IRF522, IRF523)

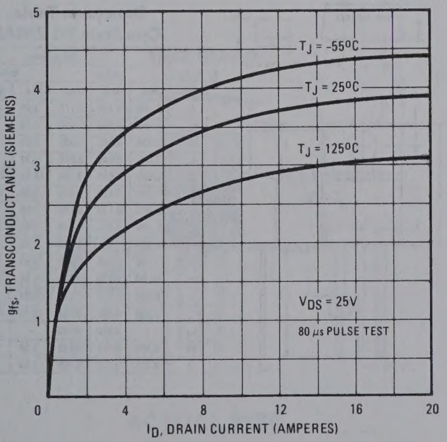


Fig 7. – Typical Transconductance Vs. Drain Current

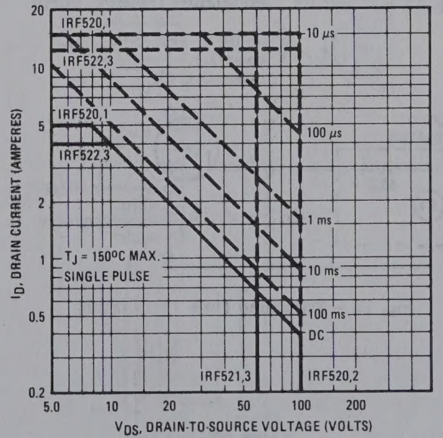


Fig. 8 – Maximum Safe Operating Area

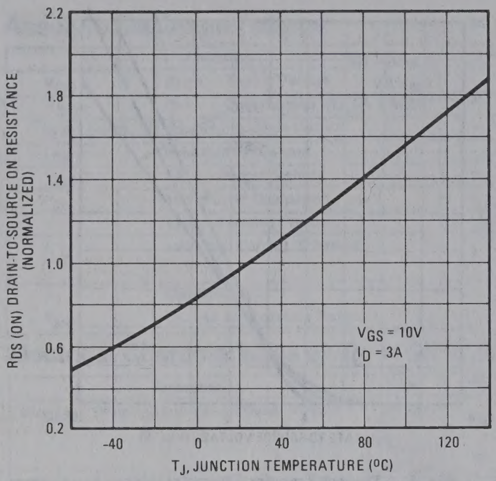


Fig. 9 — Normalized On-Resistance Vs. Temperature

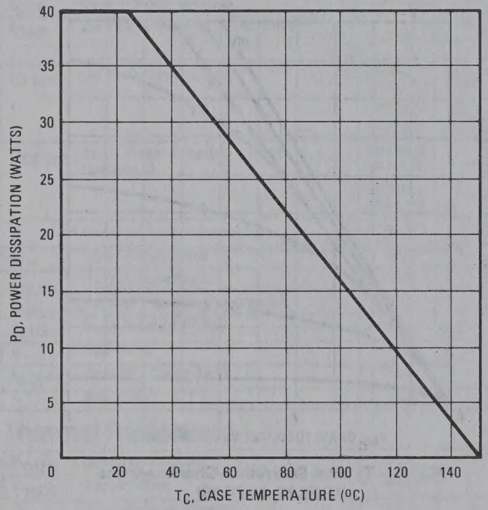


Fig. 11 — Power Vs. Temperature Derating Curve

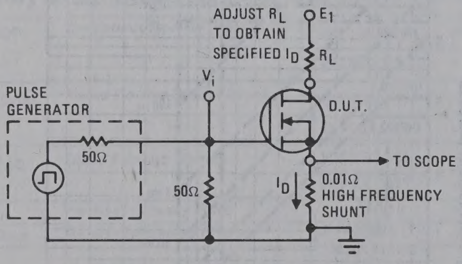


Fig. 13 — Switching Time Test Circuit

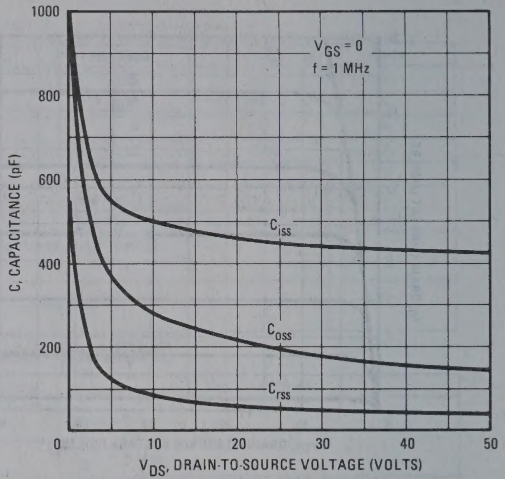


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

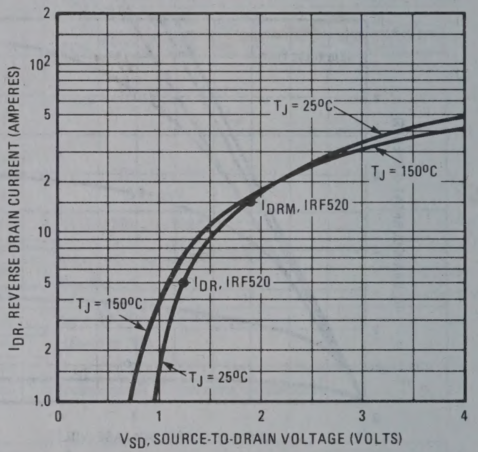
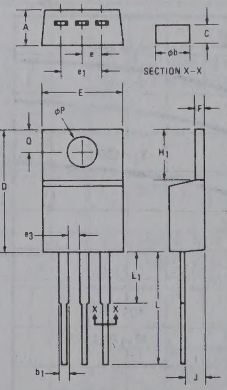


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

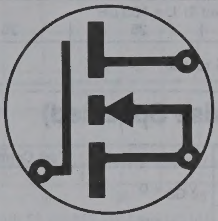


Dimension Table,
Case Style TO-220AB

Symbol	Dimensions					
	Inches			Millimeters		
	Min.	Max.	Typ.	Min.	Max.	Typ.
A	0.140	0.190	0.175	3.56	4.82	4.45
b_1	0.045	0.070	0.050	1.15	1.77	1.27
φb	0.020	0.045	0.032	0.51	1.14	0.81
C	0.012	0.045	0.018	0.31	1.14	0.46
D	0.560	0.650	0.590	14.23	16.51	14.99
E	0.380	0.420	0.400	9.66	10.66	10.16
e	0.090	0.110	0.100	2.29	2.79	2.54
e_1	0.190	0.210	0.200	4.83	5.33	5.08
e_3	0.045	–	0.050	1.15	–	1.27
F	0.020	0.055	0.050	0.51	1.39	1.27
H_1	0.230	0.270	0.248	5.85	6.85	6.30
J	0.080	0.115	0.105	2.04	2.92	2.67
L	0.500	0.580	0.550	12.70	14.73	13.98
L_1	–	0.250	0.230	–	6.35	5.84
φP	0.139	0.161	0.145	3.54	4.08	3.68
Q	0.100	0.135	0.108	2.54	3.42	2.74

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF530 IRF531 IRF532 IRF533



N Channel

100 Volt, 0.18 Ohm HEXFET™ TO-220AB Plastic Package

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

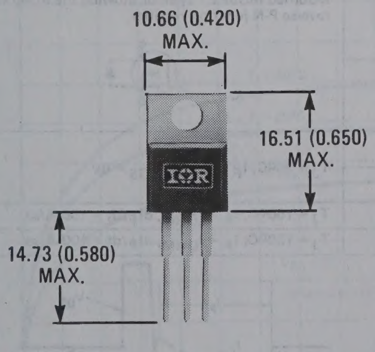
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

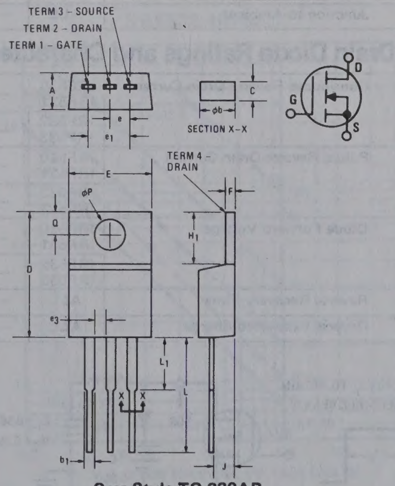
Product Summary

Part Number	V_{DS}	$R_{D\ (on)}$	I_D
IRF530	100V	0.18Ω	10A
IRF531	60V	0.18Ω	10A
IRF532	100V	0.25Ω	8A
IRF533	60V	0.25Ω	8A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB

Refer to page 166 for Case Style Dimension Table.

IRF530, IRF531, IRF532, IRF533 Devices

Absolute Maximum Ratings

Parameter		IRF530	IRF531	IRF532	IRF533	Units
V_{DS}	Drain — Source Voltage	100	60	100	60	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	100	60	100	60	V
I_D @ $T_C \cong 102^\circ C$	Continuous Drain Current	10	10	8	8	A
I_{DM}	Pulsed Drain Current	30	30	25	25	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	75 (See Fig. 11)				W
	Linear Derating Factor	0.6 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 30	30	25	25	A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				°C

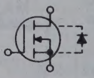
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF530 IRF532	100	—	—	V	V_{GS} = 0
		IRF531 IRF533	60	—	—	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	0.1	1.0	mA	V_{DS} = Max. Rating, V_{GS} = 0
			—	0.2	4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_J = 125°C
$I_{D\ (on)}$	On-State Drain Current	IRF530 IRF531	14	—	—	A	V_{DS} = 25V, V_{GS} = 10V
		IRF532 IRF533	12	—	—	A	
$R_{DS\ (on)}$	Static Drain-Source On State Resistance	IRF530 IRF531	—	0.14	0.18	Ω	V_{GS} = 10V, I_D = 6A
		IRF532 IRF533	—	0.20	0.25	Ω	
g_{fs}	Forward Transconductance	ALL	3.0	5.0	—	S (℧)	V_{DS} = 25V, I_D = 6A
C_{iss}	Input Capacitance	ALL	—	700	900	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	150	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	—	30	50	ns	V_{DS} = 25V, I_D = 8A
t_r	Rise Time	ALL	—	80	150	ns	(See Fig. 13)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	T_J = 125°C (MOSFET switching times are essentially
t_f	Fall Time	ALL	—	80	150	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	1.0	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF530 IRF531	—	—	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF532 IRF533	—	—	8		
I_{DRM}	Pulsed Reverse Drain Current	IRF530 IRF531	—	—	30	A	
		IRF532 IRF533	—	—	25		
V_{SD}	Diode Forward Voltage	IRF530 IRF531	—	—	2.0	V	T_J = 25°C, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF532 IRF533	—	—	1.8	V	
t_{rr}	Reverse Recovery Time	ALL	—	300	—	ns	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.0	—	μC	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

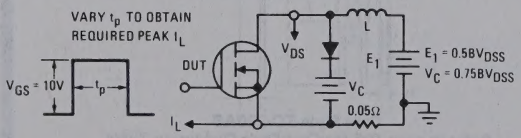


Fig. 1 — Clamped Inductive Test Circuit

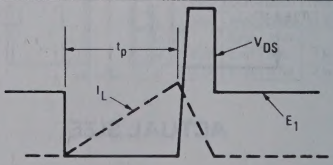


Fig. 2 — Clamped Inductive Waveforms

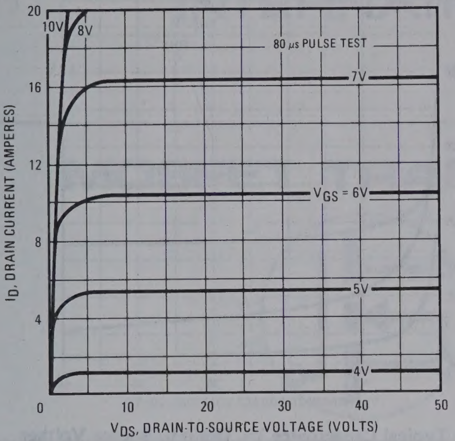


Fig. 3 — Typical Output Characteristics

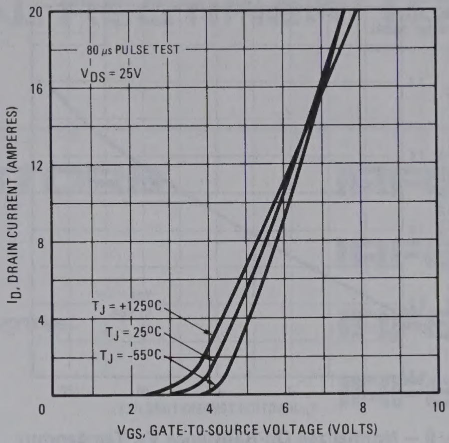


Fig. 4 — Typical Transfer Characteristics

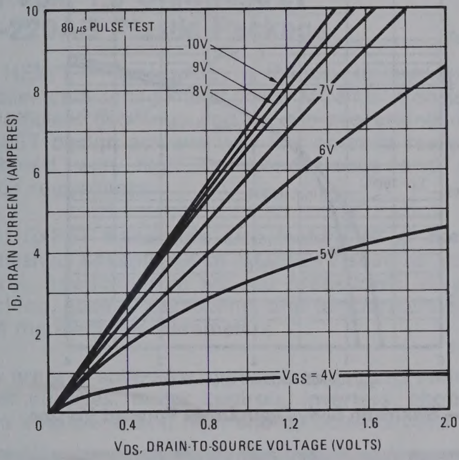


Fig. 5 — Typical Saturation Characteristics
(IRF530, IRF531)

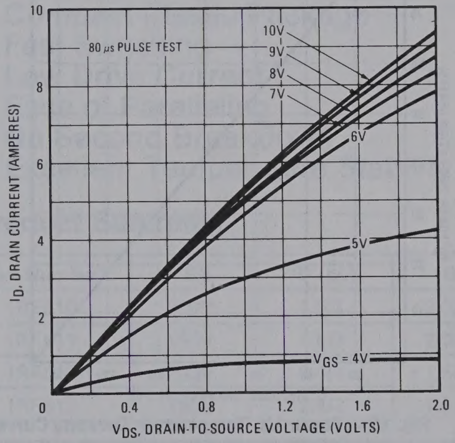


Fig. 6 — Typical Saturation Characteristics
(IRF532, IRF533)

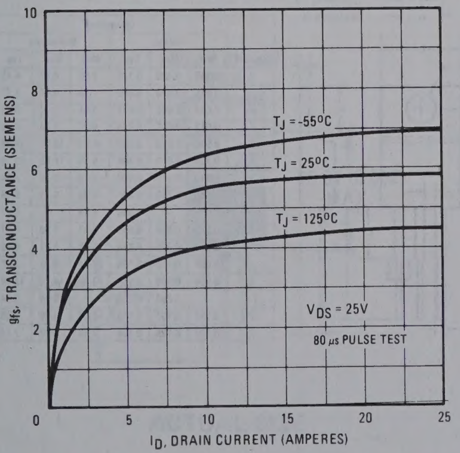


Fig 7. — Typical Transconductance Vs. Drain Current

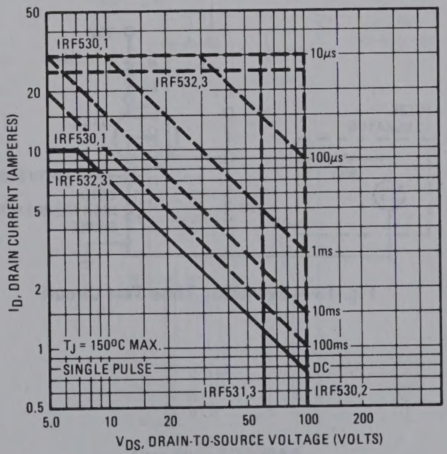


Fig. 8 — Maximum Safe Operating Area

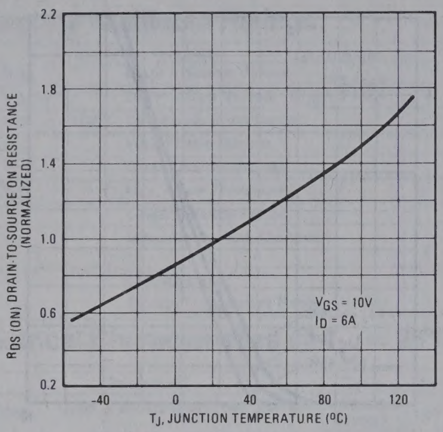


Fig. 9 — Normalized On-Resistance Vs. Temperature

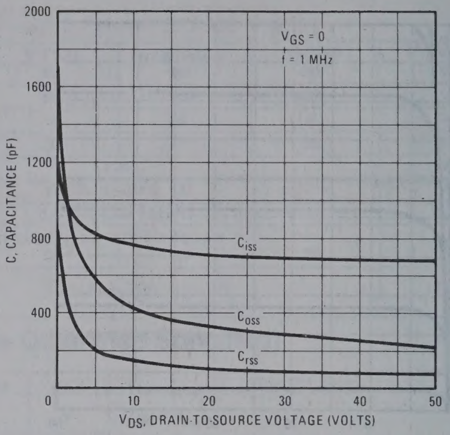


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

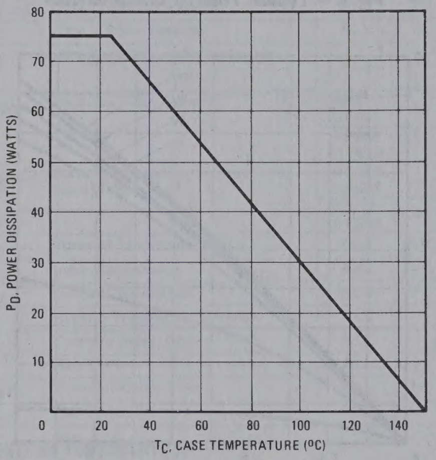


Fig. 11 — Power Vs. Temperature Derating Curve

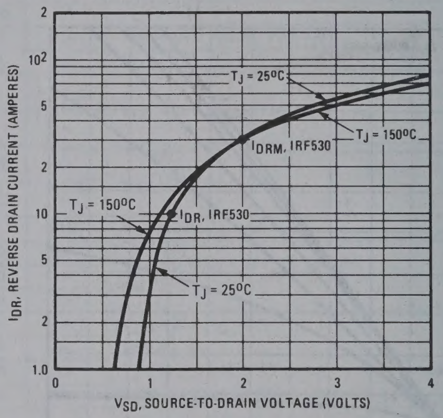


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

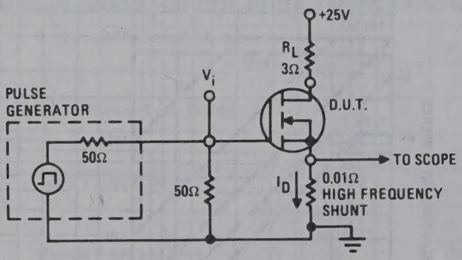
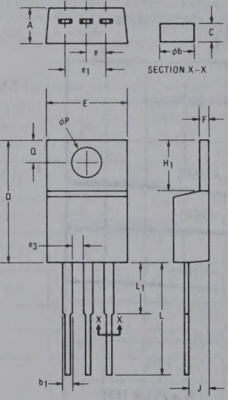


Fig. 13 — Switching Time Test Circuit



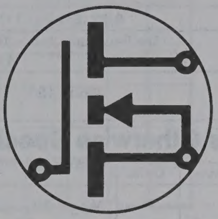
**Dimension Table,
Case Style TO-220AB**

	Dimensions					
	Inches			Millimeters		
Symbol	Min.	Max.	Typ.	Min.	Max.	Typ.
A	0.140	0.190	0.175	3.56	4.82	4.45
b_1	0.045	0.070	0.050	1.15	1.77	1.27
φb	0.020	0.045	0.032	0.51	1.14	0.81
C	0.012	0.045	0.018	0.31	1.14	0.46
D	0.560	0.650	0.590	14.23	16.51	14.99
E	0.380	0.420	0.400	9.66	10.66	10.16
e	0.090	0.110	0.100	2.29	2.79	2.54
e_1	0.190	0.210	0.200	4.83	5.33	5.08
e_3	0.045	–	0.050	1.15	–	1.27
F	0.020	0.055	0.050	0.51	1.39	1.27
H_1	0.230	0.270	0.248	5.85	6.85	6.30
J	0.080	0.115	0.105	2.04	2.92	2.67
L	0.500	0.580	0.550	12.70	14.73	13.98
L_1	–	0.250	0.230	–	6.35	5.84
φP	0.139	0.161	0.145	3.54	4.08	3.68
Q	0.100	0.135	0.108	2.54	3.42	2.74

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS

IRF610
IRF611
IRF612
IRF613



N Channel

200 Volt, 1.5 Ohm HEXFET™ TO-220AB Plastic Package

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

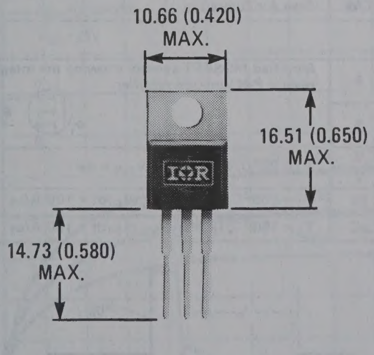
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

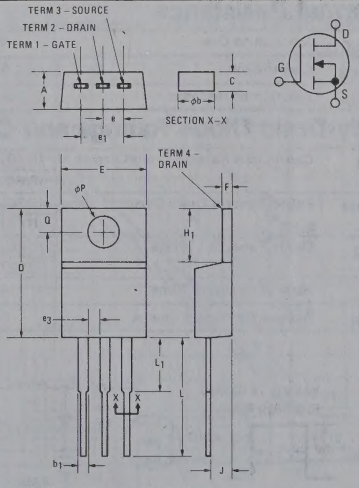
Product Summary

Part Number	V_{DS}	R_{D} (on)	I_D
IRF610	200V	1.5Ω	2.0A
IRF611	150V	1.5Ω	2.0A
IRF612	200V	2.4Ω	1.5A
IRF613	150V	2.4Ω	1.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB

Refer to page 170 for Case Style Dimension Table.

Absolute Maximum Ratings

	Parameter	IRF610	IRF611	IRF612	IRF613	Units
V_{DS}	Drain — Source Voltage	200	150	200	150	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	200	150	200	150	V
I_D @ $T_C \cong 80^oC$	Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM}	Pulsed Drain Current	5.0	5.0	4.0	4.0	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	20 (See Fig. 11)				W
	Linear Derating Factor	0.16 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH				A
		5.0	5.0	4.0	4.0	
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC

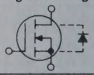
Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF610 IRF612	200	—	—	V	V_{GS} = 0V
		IRF611 IRF613	150	—	—	V	I_D = 0.5 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 0.5 mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	0.1	0.5	mA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	0.2	2.0	mA	V_{DS} = Max. Rating, V_{GS} = 0V, $T_J = 125^oC$
$I_{D\ (on)}$	On-State Drain Current	IRF610 IRF611	2.5	—	—	A	V_{DS} = 25V, V_{GS} = 10V
		IRF612 IRF613	2.0	—	—	A	
$R_{DS\ (on)}$	Static Drain-Source On State Resistance	IRF610 IRF611	—	1.0	1.5	Ω	V_{GS} = 10V, I_D = 1.0A
		IRF612 IRF613	—	1.5	2.4	Ω	
g_{fs}	Forward Transconductance	ALL	0.8	1.2	—	S (℧)	V_{DS} = 25V, I_D = 1.0A
C_{iss}	Input Capacitance	ALL	—	135	150	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	—	60	80	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	16	25	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	—	8.0	15	ns	I_D = 1A, E_1 = 0.5 BV_{DSS}, V_{GS} = 10V (See Fig. 13) $T_J = 125^oC$ (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	—	10	15	ns	
t_f	Fall Time	ALL	—	8.0	15	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	6.4	K/W	
R_{thCS}	Case-to-Sink	ALL	—	1.5	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF610, 611	—	—	2.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF612, 613	—	—	1.5		
I_{DRM}	Pulsed Reverse Drain Current	IRF610, 611	—	—	5.0	A	
		IRF612, 613	—	—	4.0		
V_{SD}	Diode Forward Voltage	IRF610, 611	—	—	2.5	V	$T_J = 25^oC$, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF612, 613	—	—	1.5	V	
t_{rr}	Reverse Recovery Time	ALL	—	200	—	ns	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	0.3	—	μC	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

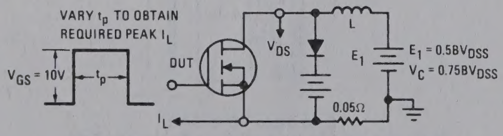


Fig. 1 — Clamped Inductive Test Circuit

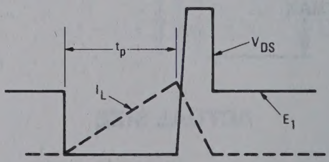


Fig. 2 — Clamped Inductive Waveforms

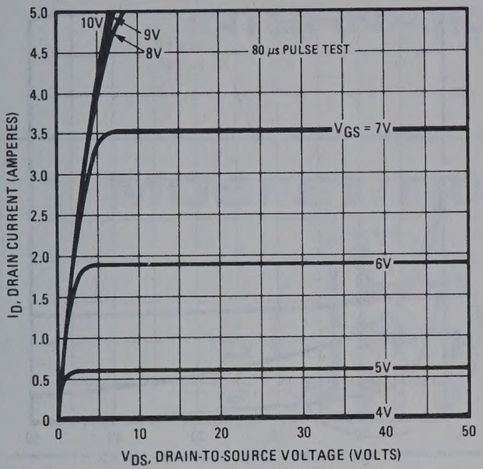


Fig. 3 – Typical Output Characteristics

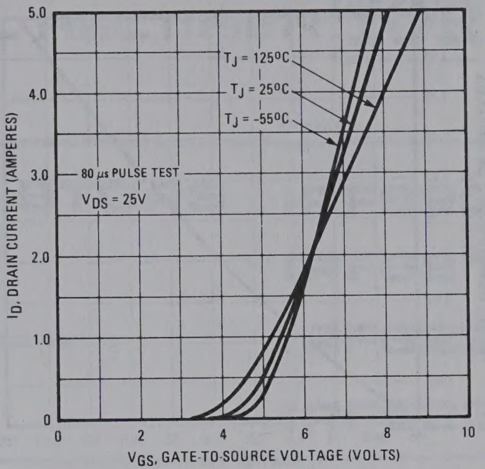


Fig. 4 – Typical Transfer Characteristics

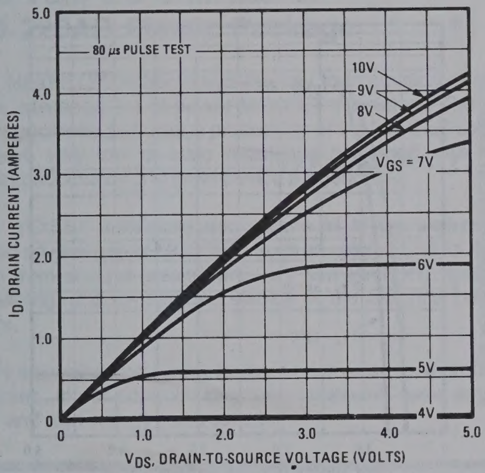


Fig. 5 – Typical Saturation Characteristics

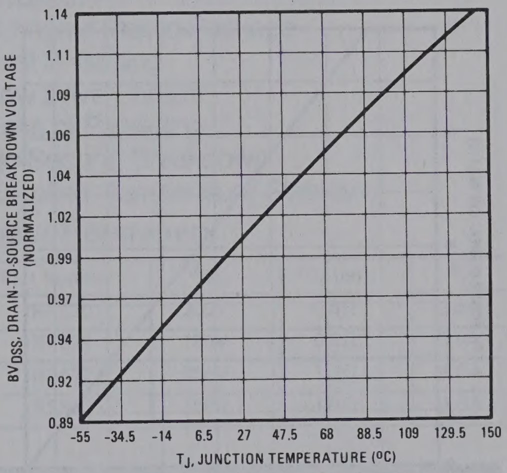


Fig. 6 – Breakdown Voltage Vs. Temperature

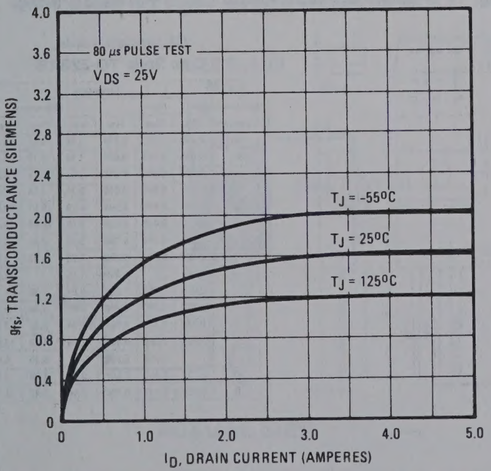


Fig. 7 – Typical Transconductance Vs. Drain Current

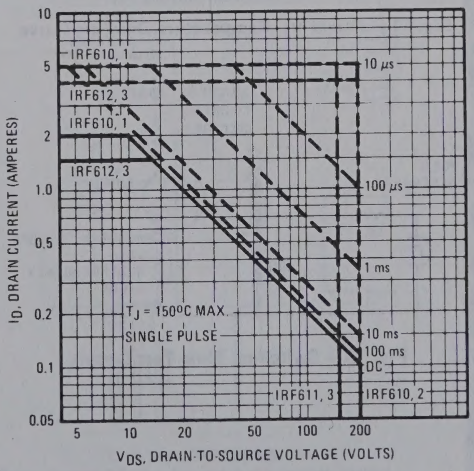


Fig. 8 – Maximum Safe Operating Area

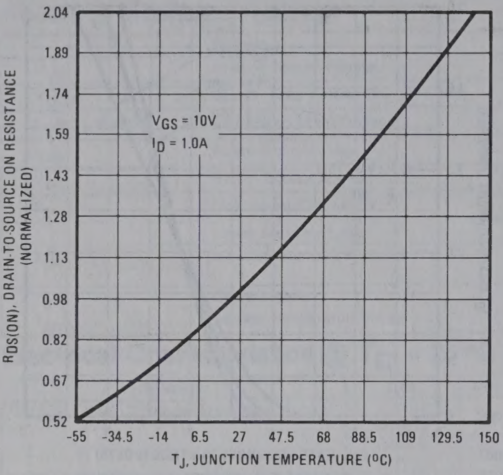


Fig. 9 – Normalized On-Resistance Vs. Temperature

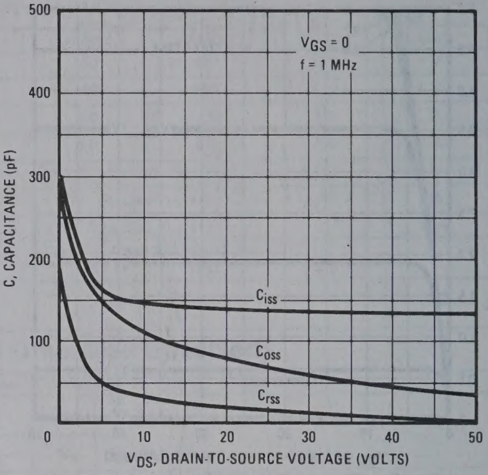


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

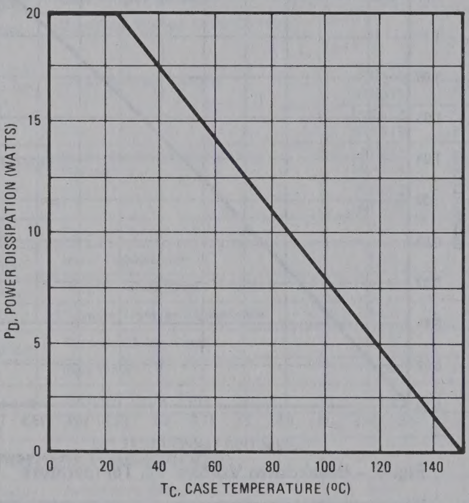


Fig. 11 – Power Vs. Temperature Derating Curve

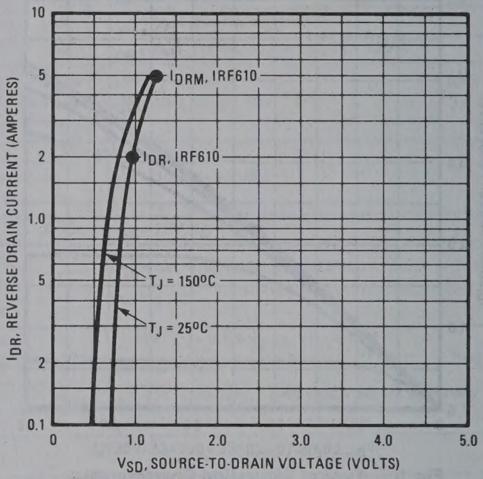


Fig. 12 – Maximum Body-Drain Diode Forward Voltage

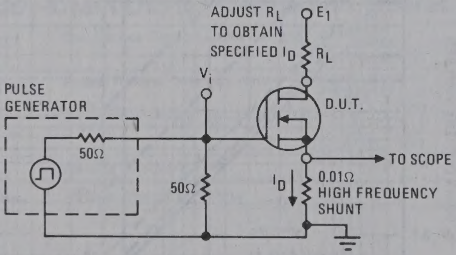
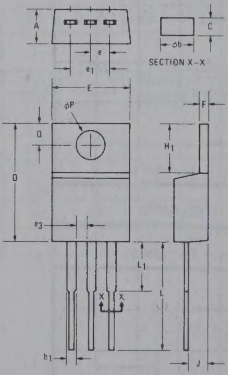


Fig. 13 – Switching Time Test Circuit



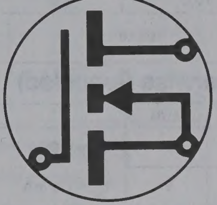
Dimension Table,
Case Style TO-220AB

Symbol	Dimensions					
	Inches			Millimeters		
	Min.	Max.	Typ.	Min.	Max.	Typ.
A	0.140	0.190	0.175	3.56	4.82	4.45
b_1	0.045	0.070	0.050	1.15	1.77	1.27
φb	0.020	0.045	0.032	0.51	1.14	0.81
C	0.012	0.045	0.018	0.31	1.14	0.46
D	0.560	0.650	0.590	14.23	16.51	14.99
E	0.380	0.420	0.400	9.66	10.66	10.16
e	0.090	0.110	0.100	2.29	2.79	2.54
e_1	0.190	0.210	0.200	4.83	5.33	5.08
e_3	0.045	–	0.050	1.15	–	1.27
F	0.020	0.055	0.050	0.51	1.39	1.27
H_1	0.230	0.270	0.248	5.85	6.85	6.30
J	0.080	0.115	0.105	2.04	2.92	2.67
L	0.500	0.580	0.550	12.70	14.73	13.98
L_1	–	0.250	0.230	–	6.35	5.84
φP	0.139	0.161	0.145	3.54	4.08	3.68
Q	0.100	0.135	0.108	2.54	3.42	2.74

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS

IRF620
IRF621
IRF622
IRF623



N Channel

200 Volt, 0.8 Ohm HEXFET™
TO-220AB Plastic Package

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

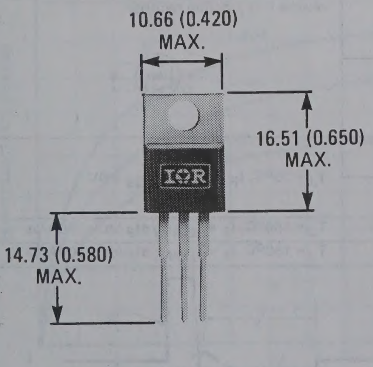
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

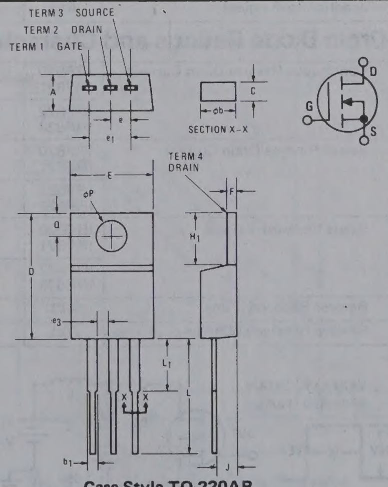
Product Summary

Part Number	V_{DS}	R_{D} (on)	I_D
IRF620	200V	0.8Ω	3.5A
IRF621	150V	0.8Ω	3.5A
IRF622	200V	1.2Ω	3.0A
IRF623	150V	1.2Ω	3.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Refer to page 174 for Case Style Dimension Table.

IRF620, IRF621, IRF622, IRF623 Devices

Absolute Maximum Ratings

Parameter		IRF620	IRF621	IRF622	IRF623	Units
V_{DS}	Drain — Source Voltage	200	150	200	150	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	200	150	200	150	V
I_D @ $T_C \cong 96.5^oC$	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current	10.0	10.0	8.0	8.0	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	40 (See Fig. 11)				W
	Linear Derating Factor	0.32 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 µH				A
		10.0	10.0	8.0	8.0	
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC

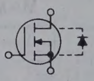
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF620 IRF622	200	—	—	V	V_{GS} = 0V
		IRF621 IRF623	150	—	—	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	0.1	1.0	mA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	0.2	4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0V, T_J = 125°C
$I_{D\ (on)}$	On-State Drain Current	IRF620 IRF621	5.0	—	—	A	V_{DS} = 25V, V_{GS} = 10V
		IRF622 IRF623	4.0	—	—	A	
$R_{DS\ (on)}$	Static Drain-Source On State Resistance	IRF620 IRF621	—	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.0A
		IRF622 IRF623	—	0.8	1.2	Ω	
g_{fs}	Forward Transconductance	ALL	1.3	2.3	—	S (℧)	V_{DS} = 25V, I_D = 2.0A
C_{iss}	Input Capacitance	ALL	—	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	—	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	40	80	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	—	20	40	ns	I_D = 2A, E_1 = 0.5 BV_{DSS} (See Fig. 13) T_J = 125°C (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	30	60	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	30	60	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	1.0	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF620 IRF621	—	—	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF622 IRF623	—	—	3.0		
I_{DRM}	Pulsed Reverse Drain Current	IRF620 IRF621	—	—	10.0	A	
		IRF622 IRF623	—	—	8.0		
V_{SD}	Diode Forward Voltage	IRF620 IRF621	—	—	1.57	V	T_J = 25°C, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF622 IRF623	—	—	1.44	V	
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100A/µs
Q_{RR}	Reverse Recovered Charge	ALL	—	6.0	—	µC	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100A/µs

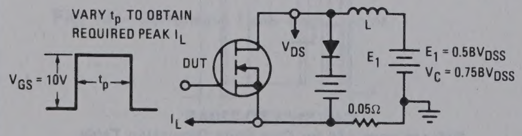


Fig. 1 — Clamped Inductive Test Circuit

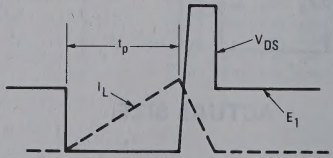


Fig. 2 — Clamped Inductive Waveforms

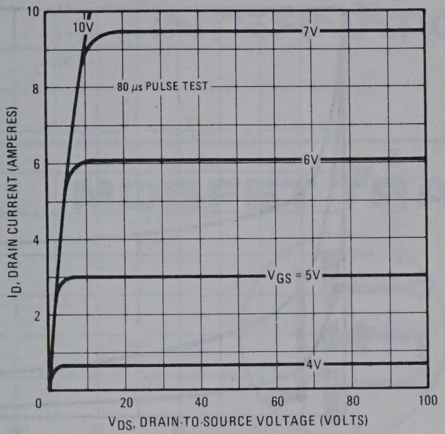


Fig. 3 — Typical Output Characteristics

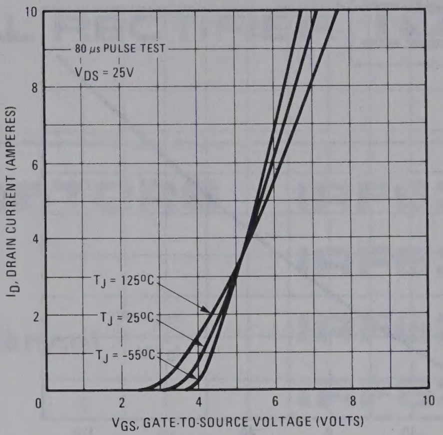


Fig. 4 — Typical Transfer Characteristics

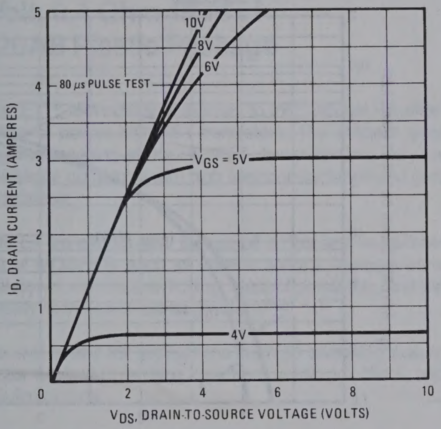


Fig. 5 — Typical Saturation Characteristics (IRF620, IRF621)

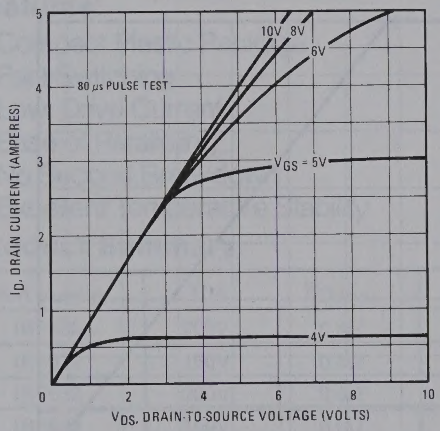


Fig. 6 — Typical Saturation Characteristics (IRF622, IRF623)

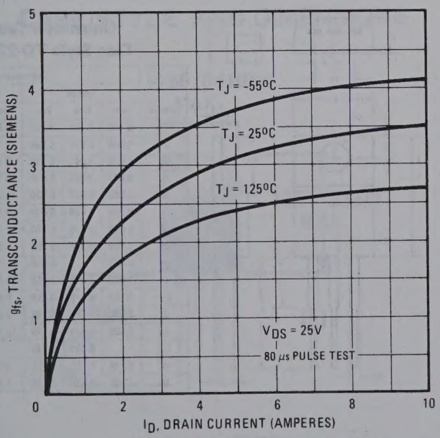


Fig 7. — Typical Transconductance Vs. Drain Current

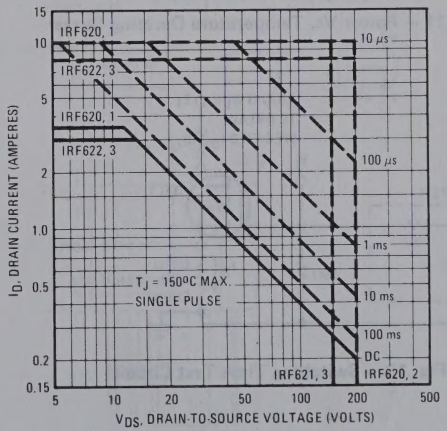


Fig. 8 — Maximum Safe Operating Area

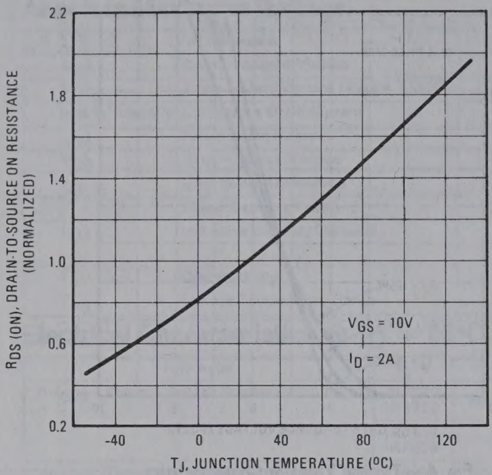


Fig. 9 – Normalized On-Resistance Vs. Temperature

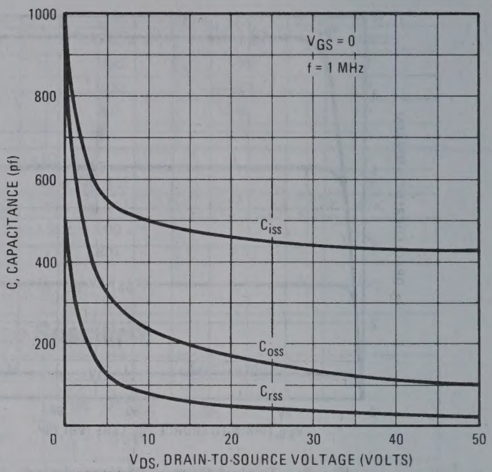


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

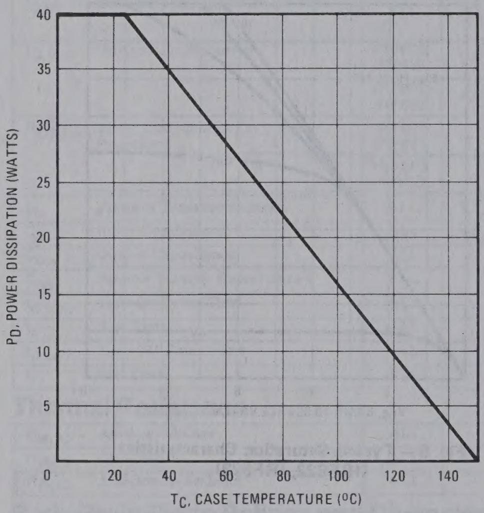


Fig. 11 – Power Vs. Temperature Derating Curve

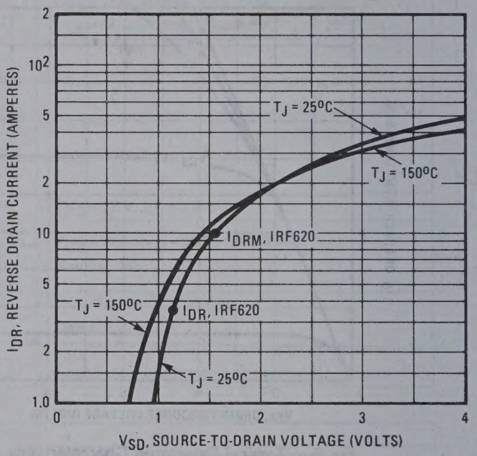
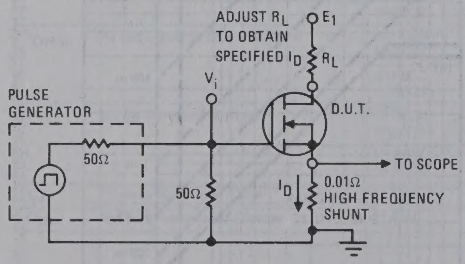
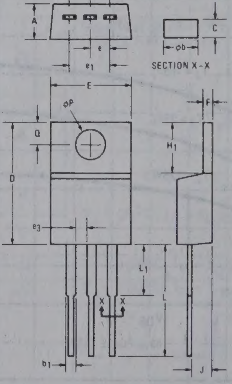


Fig. 12 – Maximum Body-Drain Diode Forward Voltage



ADJUST R_L TO OBTAIN SPECIFIED I_D
E_1
R_L
V_i
PULSE GENERATOR
50Ω
50Ω
D.U.T.
TO SCOPE
I_D
0.01Ω HIGH FREQUENCY SHUNT

Fig. 13 – Switching Time Test Circuit

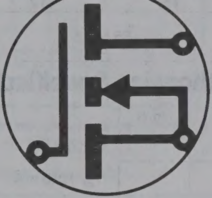


Dimension Table, Case Style TO-220AB

Symbol	Dimensions					
	Inches			Millimeters		
	Min.	Max.	Typ.	Min.	Max.	Typ.
A	0.140	0.190	0.175	3.56	4.82	4.45
b_1	0.045	0.070	0.050	1.15	1.77	1.27
φb	0.020	0.045	0.032	0.51	1.14	0.81
C	0.012	0.045	0.018	0.31	1.14	0.46
D	0.560	0.650	0.590	14.23	16.51	14.99
E	0.380	0.420	0.400	9.66	10.66	10.16
e	0.090	0.110	0.100	2.29	2.79	2.54
e_1	0.190	0.210	0.200	4.83	5.33	5.08
e_3	0.045	–	0.050	1.15	–	1.27
F	0.020	0.055	0.050	0.51	1.39	1.27
H_1	0.230	0.270	0.248	5.85	6.85	6.30
J	0.080	0.115	0.105	2.04	2.92	2.67
L	0.500	0.580	0.550	12.70	14.73	13.98
L_1	–	0.250	0.230	–	6.35	5.84
φP	0.139	0.161	0.145	3.54	4.08	3.68
Q	0.100	0.135	0.108	2.54	3.42	2.74

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF630 IRF631 IRF632 IRF633



N Channel

200 Volt, 0.4 Ohm HEXFET™ TO-220AB Plastic Package

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

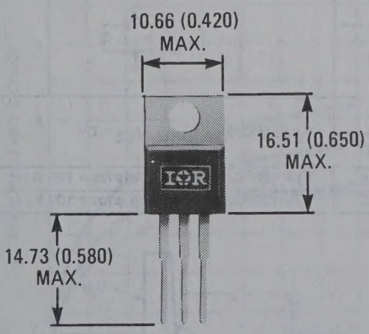
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

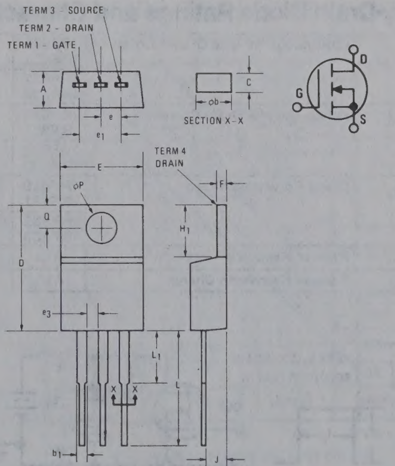
Product Summary

Part Number	V_{DS}	$R_{D\ (on)}$	I_D
IRF630	200V	0.4Ω	6A
IRF631	150V	0.4Ω	6A
IRF632	200V	0.6Ω	5A
IRF633	150V	0.6Ω	5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB

Refer to page 178 for Case Style Dimension Table.

IRF630, IRF631, IRF632, IRF633 Devices

Absolute Maximum Ratings

Parameter		IRF630	IRF631	IRF632	IRF633	Units
V_{DS}	Drain – Source Voltage	200	150	200	150	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	200	150	200	150	V
I_D @ $T_C \cong 102^\circ C$	Continuous Drain Current	6	6	5	5	A
I_{DM}	Pulsed Drain Current	15	15	12	12	A
V_{GS}	Gate – Source Voltage	±20				V
P_D	Max. Power Dissipation	75 (See Fig. 11)				W
	Linear Derating Factor	0.6 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 15	15	12	12	A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				°C

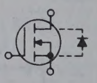
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRF630 IRF632	200	–	–	V	V_{GS} = 0V
		IRF631 IRF633	150	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate – Body Leakage	ALL	–	–	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0	mA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	0.2	4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0V, T_J = 125°C
$I_{D\ (on)}$	On-State Drain Current	IRF630 IRF631	9.0	–	–	A	V_{DS} = 25V, V_{GS} = 10V
		IRF632 IRF633	8.0	–	–	A	
$R_{DS\ (on)}$	Static Drain-Source On State Resistance	IRF630 IRF631	–	0.25	0.4	Ω	V_{GS} = 10V, I_D = 3.5A
		IRF632 IRF633	–	0.4	0.6	Ω	
g_{fs}	Forward Transconductance	ALL	2.5	4.5	–	S (℧)	V_{DS} = 25V, I_D = 3.5A
C_{iss}	Input Capacitance	ALL	–	700	900	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	–	250	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	150	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	30	50	ns	I_D = 4A, E_1 = 0.5 BV_{DSS} (See Fig. 13) T_J = 125°C (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	70	140	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	70	140	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	–	1.0	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF630 IRF631	–	–	6	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF632 IRF633	–	–	5		
I_{DRM}	Pulsed Reverse Drain Current	IRF630 IRF631	–	–	15	A	
		IRF632 IRF633	–	–	12		
V_{SD}	Diode Forward Voltage	IRF630 IRF631	–	–	1.45	V	T_J = 25°C, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF632 IRF633	–	–	1.31	V	
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10.0	–	μC	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

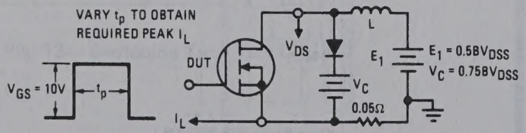


Fig. 1 – Clamped Inductive Test Circuit

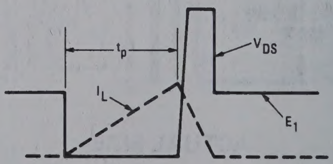


Fig. 2 – Clamped Inductive Waveforms

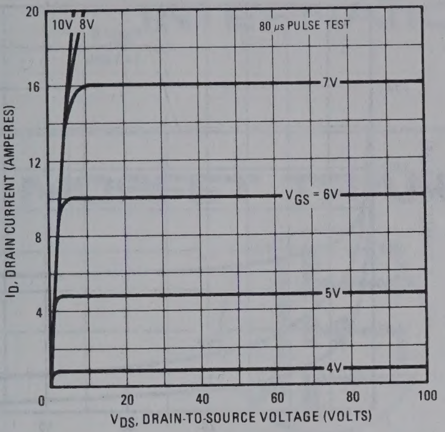


Fig. 3 — Typical Output Characteristics

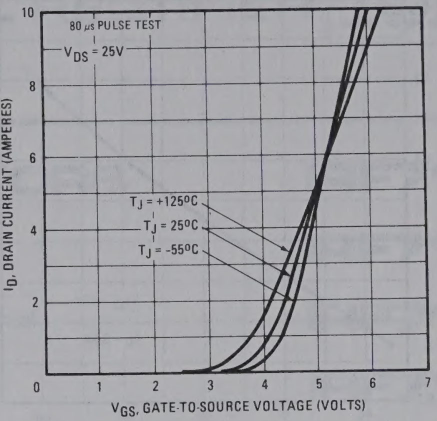


Fig. 4 — Typical Transfer Characteristics

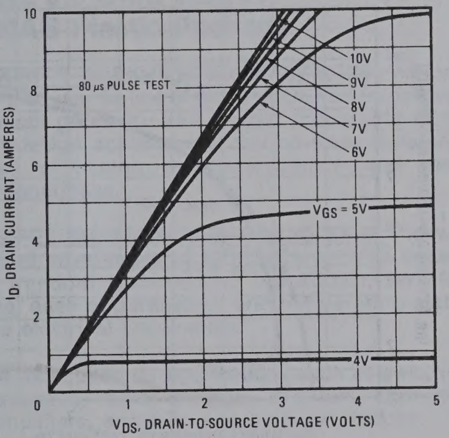


Fig. 5 — Typical Saturation Characteristics (IRF630, IRF631)

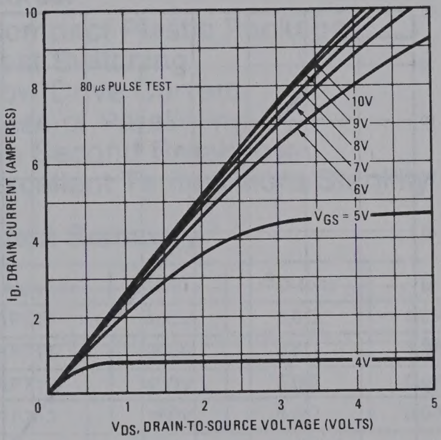


Fig. 6 — Typical Saturation Characteristics (IRF632, IRF633)

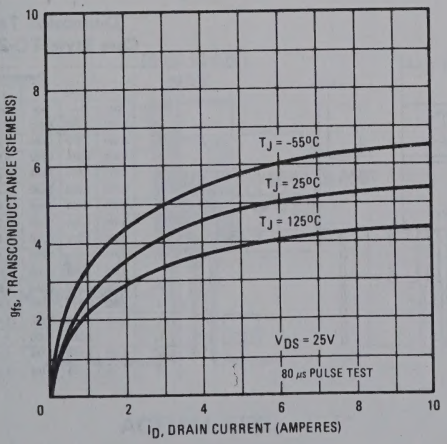


Fig. 7 — Typical Transconductance Vs. Drain Current

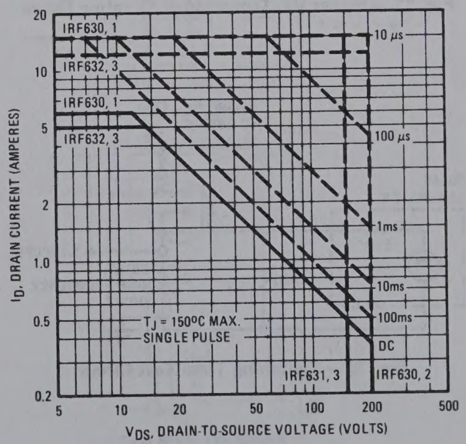


Fig. 8 — Maximum Safe Operating Area

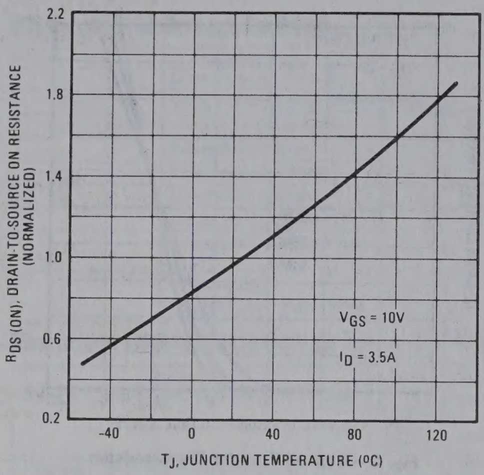


Fig. 9 — Normalized On-Resistance Vs. Temperature

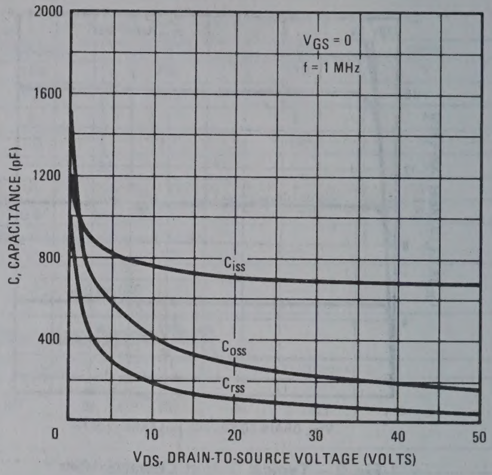


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

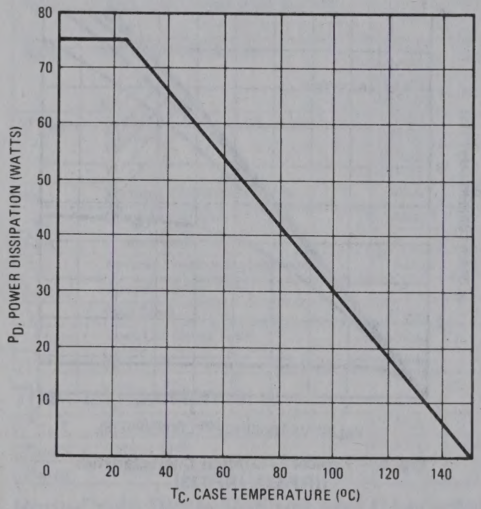


Fig. 11 — Power Vs. Temperature Derating Curve

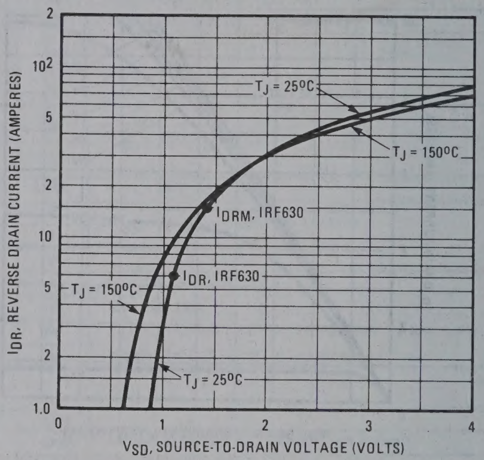


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

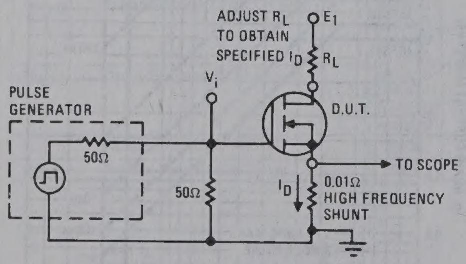
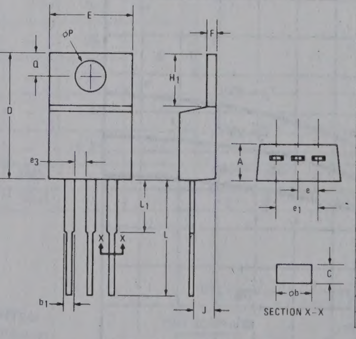


Fig. 13 — Switching Time Test Circuit



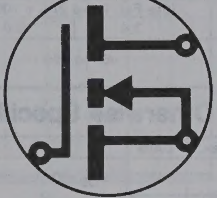
Dimension Table, Case Style TO-220AB

	Dimensions					
	Inches			Millimeters		
Symbol	Min.	Max.	Typ.	Min.	Max.	Typ.
A	0.140	0.190	0.175	3.56	4.82	4.45
b_1	0.045	0.070	0.050	1.15	1.77	1.27
ϕb	0.020	0.045	0.032	0.51	1.14	0.81
C	0.012	0.045	0.018	0.31	1.14	0.46
D	0.560	0.650	0.590	14.23	16.51	14.99
E	0.380	0.420	0.400	9.66	10.66	10.16
e	0.090	0.110	0.100	2.29	2.79	2.54
e_1	0.190	0.210	0.200	4.83	5.33	5.08
e_3	0.045	–	0.050	1.15	–	1.27
F	0.020	0.055	0.050	0.51	1.39	1.27
H_1	0.230	0.270	0.248	5.85	6.85	6.30
J	0.080	0.115	0.105	2.04	2.92	2.67
L	0.500	0.580	0.550	12.70	14.73	13.98
L_1	–	0.250	0.230	–	6.35	5.84
ϕP	0.139	0.161	0.145	3.54	4.08	3.68
Q	0.100	0.135	0.108	2.54	3.42	2.74

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS

IRF710
IRF711
IRF712
IRF713



N Channel

400 Volt, 3.6 Ohm HEXFET™ TO-220AB Plastic Package

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

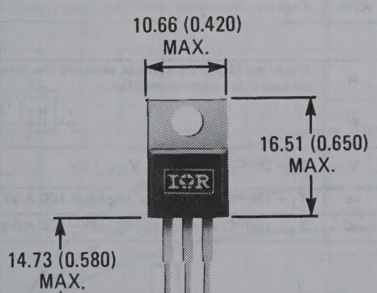
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

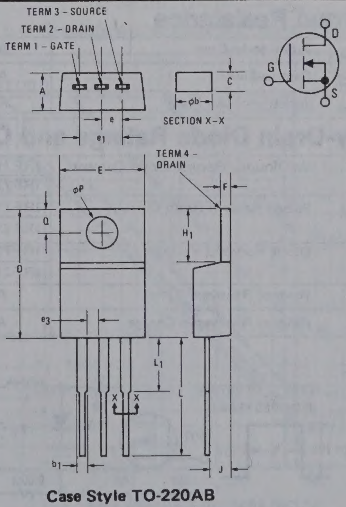
Product Summary

Part Number	V_{DS}	R_{D} (on)	I_D
IRF710	400V	3.6Ω	1.2A
IRF711	350V	3.6Ω	1.2A
IRF712	400V	5.0Ω	0.9A
IRF713	350V	5.0Ω	0.9A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB

Refer to page 182 for Case Style Dimension Table.

Absolute Maximum Ratings

	Parameter	IRF710	IRF711	IRF712	IRF713	Units
V_{DS}	Drain — Source Voltage	400	350	400	350	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	400	350	400	350	V
I_D @ $T_C \cong 80^oC$	Continuous Drain Current	1.2	1.2	0.9	0.9	A
I_{DM}	Pulsed Drain Current	2.4	2.4	2.0	2.0	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	20 (See Fig. 11)				W
	Linear Derating Factor	0.16 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 2.4	2.4	2.0	2.0	A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC

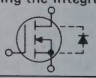
Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS} Drain — Source Breakdown Voltage	IRF710 IRF712	400	–	–	V	$V_{GS} = 0$
	IRF711 IRF713	350	–	–	V	I_D = 0.5 mA
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, I_D = 0.5 mA
I_{GSS} Gate — Body Leakage	ALL	–	–	500	nA	V_{GS} = 20V
I_{DSS} Zero Gate Voltage Drain Current	ALL	–	0.1	0.5	mA	V_{DS} = Max. Rating, $V_{GS} = 0$
		–	0.2	2.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_J = 125^oC$
$I_{D\ (on)}$ On-State Drain Current	IRF710 IRF711	1.6	–	–	A	V_{DS} = 25V, V_{GS} = 10V
	IRF712 IRF713	1.3	–	–	A	
$R_{DS\ (on)}$ Static Drain-Source On State Resistance	IRF710 IRF711	–	3.3	3.6	Ω	V_{GS} = 10V, I_D = 0.6A
	IRF712 IRF713	–	3.6	5.0	Ω	
g_{fs} Forward Transconductance	ALL	0.5	1.0	–	S (℧)	V_{DS} = 100V, I_D = 0.6A
C_{iss} Input Capacitance	ALL	–	135	150	pF	$V_{GS} = 0$, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss} Output Capacitance	ALL	–	35	50	pF	
C_{rss} Reverse Transfer Capacitance	ALL	–	8.0	15	pF	
$t_{d\ (on)}$ Turn-On Delay Time	ALL	–	3.0	10	ns	I_D = 0.6A, $E_1 = 0.5\ BV_{DSS}$, V_{GS} = 10V (See Fig. 13) $T_J = 125^oC$ (MOSFET Switching times are essentially independent of operating temperature.)
t_r Rise Time	ALL	–	10	20	ns	
$t_{d\ (off)}$ Turn-Off Delay Time	ALL	–	5.0	10	ns	
t_f Fall Time	ALL	–	8.0	15	ns	

Thermal Resistance

R_{thJC} Junction-to-Case	ALL	–	–	6.4	K/W	
R_{thCS} Case-to-Sink	ALL	–	1.5	–	K/W	Mounting surface flat, smooth, and greased
R_{thJA} Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR} Continuous Reverse Drain Current	IRF710, 711	–	–	1.2	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	IRF712, 713	–	–	0.9		
I_{DRM} Pulsed Reverse Drain Current	IRF710, 711	–	–	2.4	A	
	IRF712, 713	–	–	2.0		
V_{SD} Diode Forward Voltage	IRF710, 711	–	–	1.30	V	$T_J = 25^oC$, $I_F = I_{DRM}$, V_{GS} = 0V
	IRF712, 713	–	–	1.25		
t_{rr} Reverse Recovery Time	ALL	–	250	–	ns	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR} Reverse Recovered Charge	ALL	–	0.15	–	μC	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

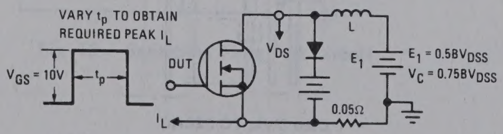


Fig. 1 — Clamped Inductive Test Circuit

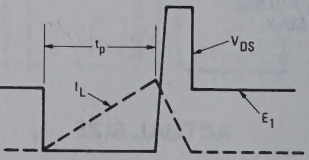


Fig. 2 — Clamped Inductive Waveforms

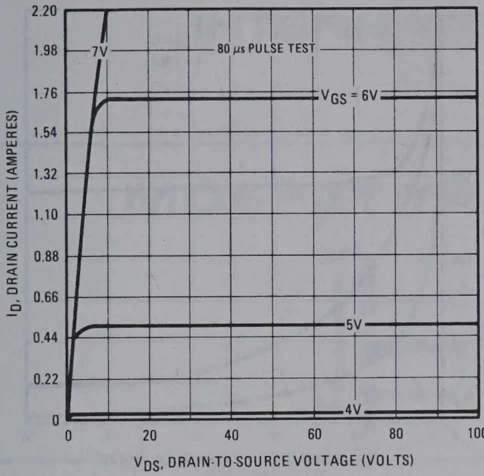


Fig. 3 – Typical Output Characteristics

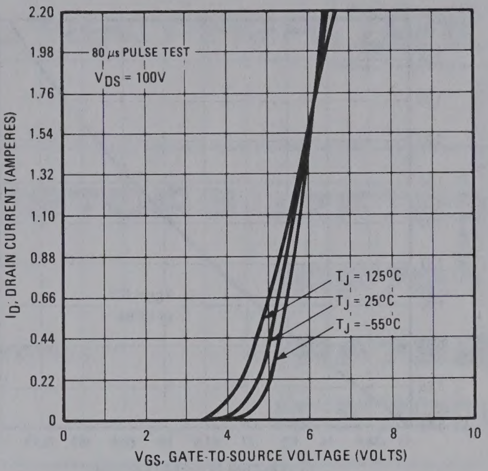


Fig. 4 – Typical Transfer Characteristics

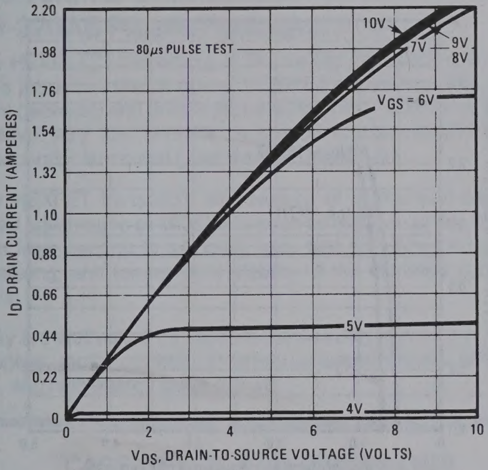


Fig. 5 – Typical Saturation Characteristics

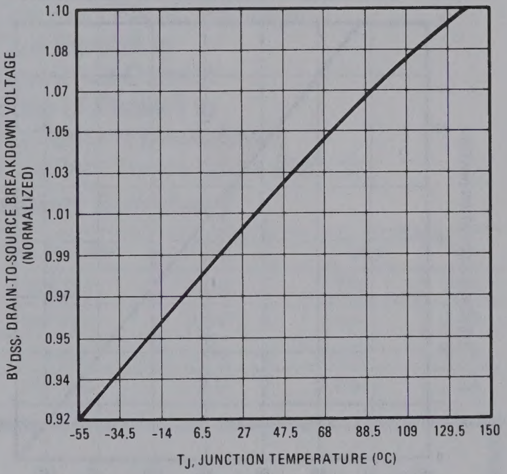


Fig. 6 – Breakdown Voltage Vs. Temperature

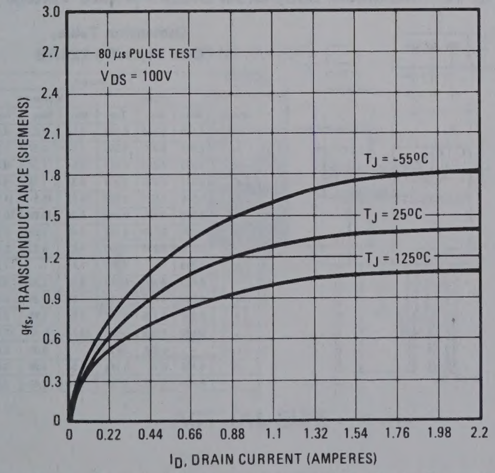


Fig. 7 – Typical Transconductance Vs. Drain Current

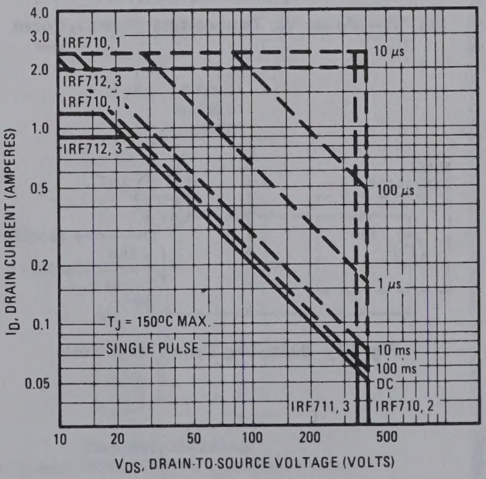


Fig. 8 – Maximum Safe Operating Area

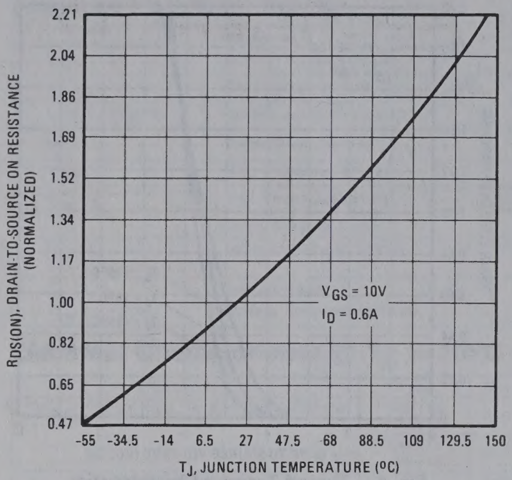


Fig. 9 — Normalized On-Resistance Vs. Temperature

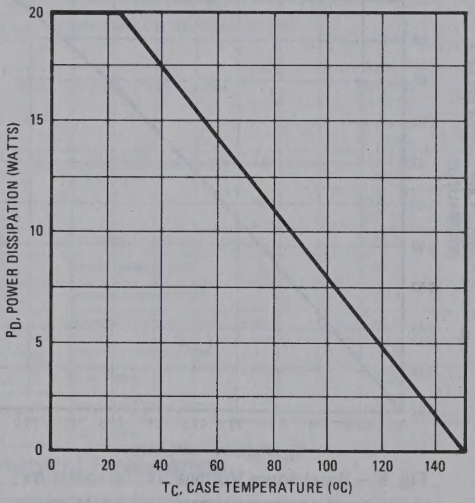


Fig. 11 — Power Vs. Temperature Derating Curve

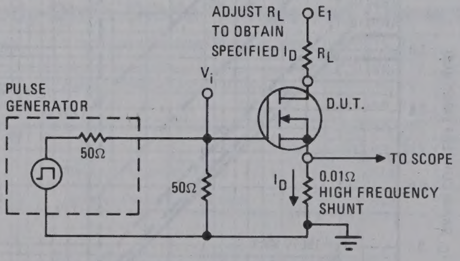

ADJUST R_L TO OBTAIN SPECIFIED I_D
E_1
R_L
V_i
PULSE GENERATOR
50Ω
D.U.T.
TO SCOPE
50Ω
I_D
0.01Ω HIGH FREQUENCY SHUNT

Fig. 13 — Switching Time Test Circuit

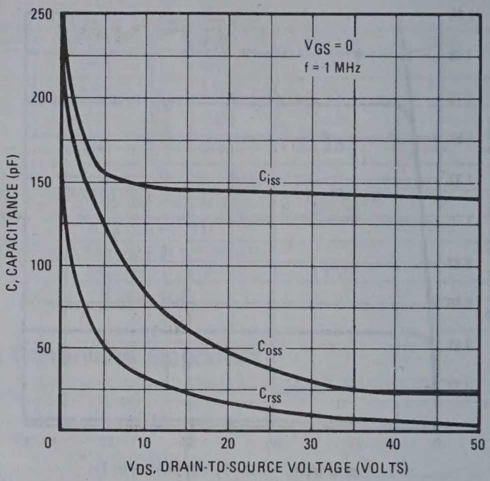


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

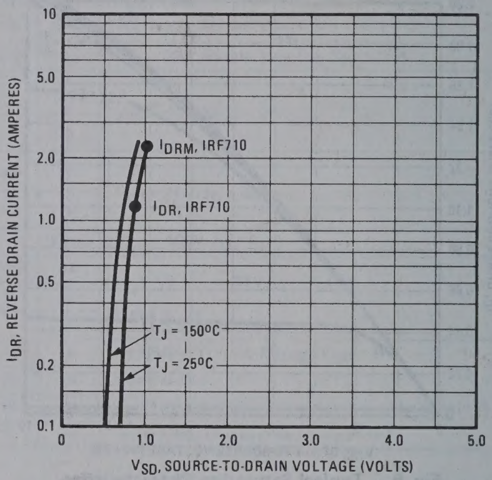
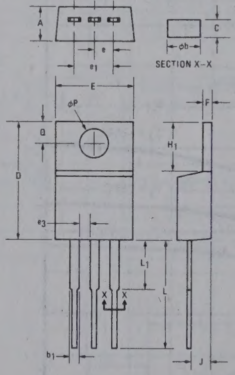


Fig. 12 — Maximum Body-Drain Diode Forward Voltage



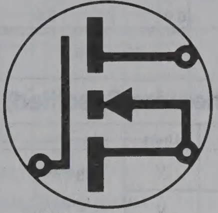
Dimension Table, Case Style TO-220AB

	Dimensions					
	Inches			Millimeters		
Symbol	Min.	Max.	Typ.	Min.	Max.	Typ.
A	0.140	0.190	0.175	3.56	4.82	4.45
b_1	0.045	0.070	0.050	1.15	1.77	1.27
ϕb	0.020	0.045	0.032	0.51	1.14	0.81
C	0.012	0.045	0.018	0.31	1.14	0.46
D	0.560	0.650	0.590	14.23	16.51	14.99
E	0.380	0.420	0.400	9.66	10.66	10.16
e	0.090	0.110	0.100	2.29	2.79	2.54
e_1	0.190	0.210	0.200	4.83	5.33	5.08
e_3	0.045	–	0.050	1.15	–	1.27
F	0.020	0.055	0.050	0.51	1.39	1.27
H_1	0.230	0.270	0.248	5.85	6.85	6.30
J	0.080	0.115	0.105	2.04	2.92	2.67
L	0.500	0.580	0.550	12.70	14.73	13.98
L_1	–	0.250	0.230	–	6.35	5.84
ϕP	0.139	0.161	0.145	3.54	4.08	3.68
Q	0.100	0.135	0.108	2.54	3.42	2.74

PD-9.315

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF720 IRF721 IRF722 IRF733



N Channel

400 Volt, 1.8 Ohm HEXFET™ TO-220AB Plastic Package

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They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

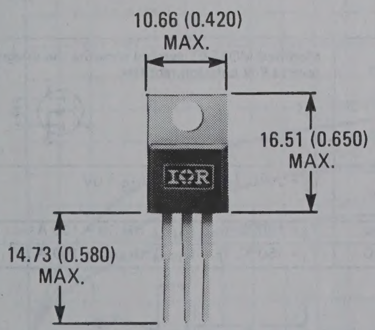
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

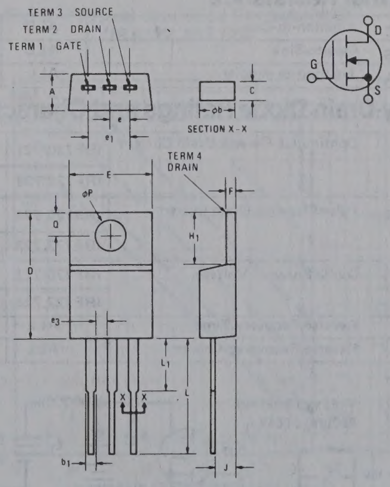
Product Summary

Part Number	V_{DS}	$R_{D\ (on)}$	I_D
IRF720	400V	1.8Ω	2.5A
IRF721	350V	1.8Ω	2.5A
IRF722	400V	2.5Ω	2.0A
IRF723	350V	2.5Ω	2.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB

Refer to page 186 for Case Style Dimension Table.

IRF720, IRF721, IRF722, IRF723 Devices

Absolute Maximum Ratings

Parameter		IRF720	IRF721	IRF722	IRF723	Units
V_{DS}	Drain — Source Voltage	400	350	400	350	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	400	350	400	350	V
I_D @ $T_C \cong 96.5^oC$	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_{DM}	Pulsed Drain Current	6.0	6.0	5.0	5.0	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	40 (See Fig. 11)				W
	Linear Derating Factor	0.32 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH				A
		6.0	6.0	5.0	5.0	
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC

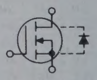
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF720 IRF722	400	—	—	V	$V_{GS} = 0$
		IRF721 IRF723	350	—	—	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	0.1	1.0	mA	V_{DS} = Max. Rating, V_{GS} = 0
			—	0.2	4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0, $T_J = 125^oC$
$I_{D\ (on)}$	On-State Drain Current	IRF720 IRF721	3.0	—	—	A	V_{DS} = 25V, V_{GS} = 10V
		IRF722 IRF723	2.5	—	—	A	
$R_{DS\ (on)}$	Static Drain-Source On State Resistance	IRF720 IRF721	—	1.5	1.8	Ω	V_{GS} = 10V, I_D = 1.5A
		IRF722 IRF723	—	1.8	2.5	Ω	
g_{fs}	Forward Transconductance	ALL	1.0	2.0	—	S (℧)	V_{DS} = 100V, I_D = 1.5A
C_{iss}	Input Capacitance	ALL	—	450	600	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	—	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	40	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	—	20	40	ns	I_D = 1.5A, E_1 = 0.5 BV_{DSS} (See Fig. 13) $T_J = 125^oC$ (MOSFET Switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	25	50	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	25	50	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	1.0	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF720, 721	—	—	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF722, 723	—	—	2.0		
I_{DRM}	Pulsed Reverse Drain Current	IRF720, 721	—	—	6.0	A	
		IRF722, 723	—	—	5.0		
V_{SD}	Diode Forward Voltage	IRF720, 721	—	—	1.30	V	$T_J = 25^oC$, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF722, 723	—	—	1.25		
t_{rr}	Reverse Recovery Time	ALL	—	400	—	ns	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	5.0	—	μC	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

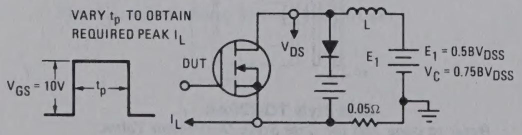


Fig. 1 — Clamped Inductive Test Circuit

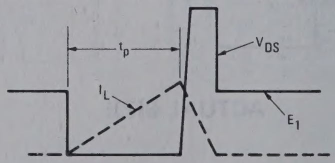


Fig. 2 — Clamped Inductive Waveforms

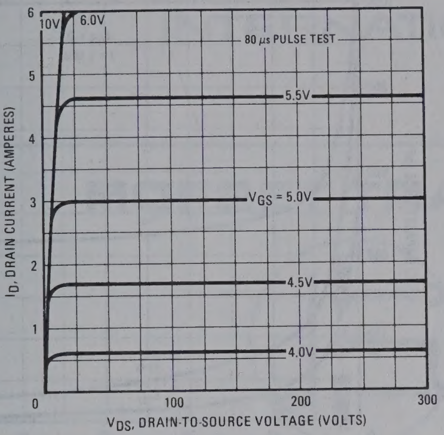


Fig. 3 – Typical Output Characteristics

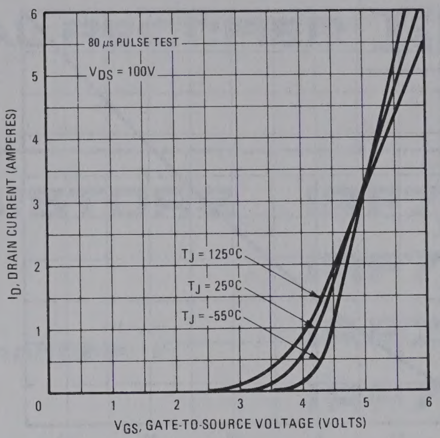


Fig. 4 – Typical Transfer Characteristics

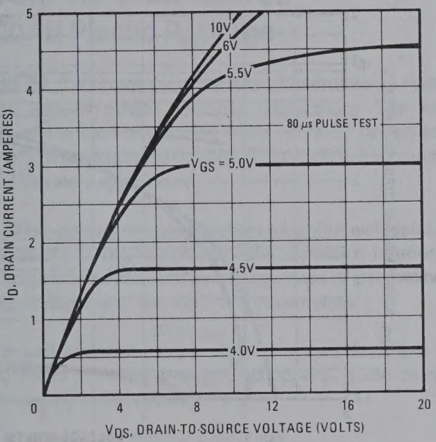


Fig. 5 – Typical Saturation Characteristics
(IRF720, IRF721)

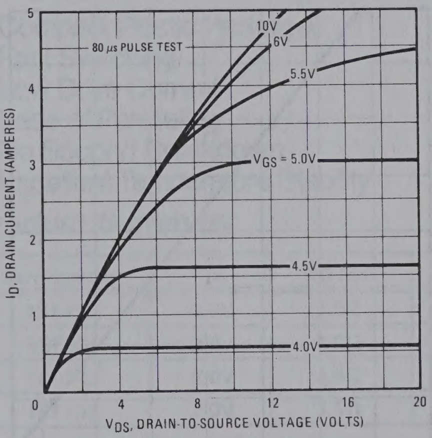


Fig. 6 – Typical Saturation Characteristics
(IRF722, IRF723)

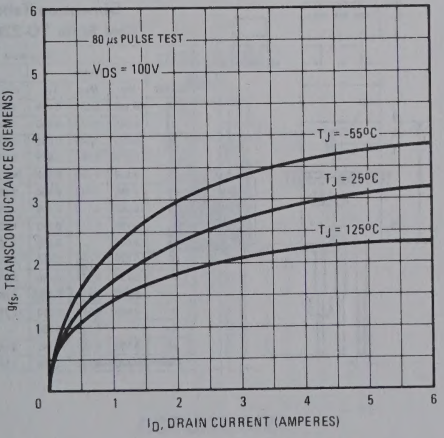


Fig. 7 – Typical Transconductance Vs. Drain Current

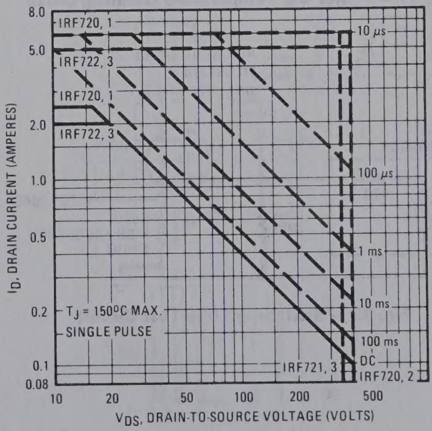


Fig. 8 – Maximum Safe Operating Area

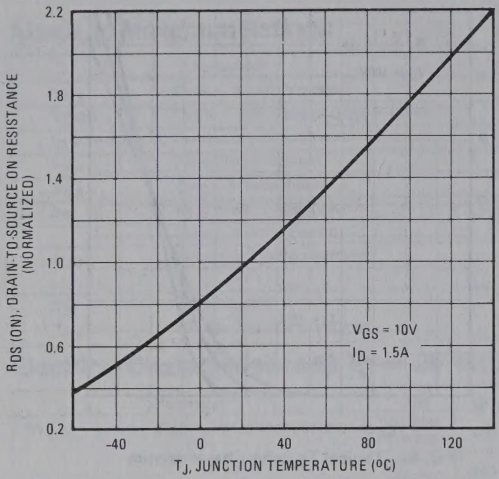


Fig. 9 – Normalized On-Resistance Vs. Temperature

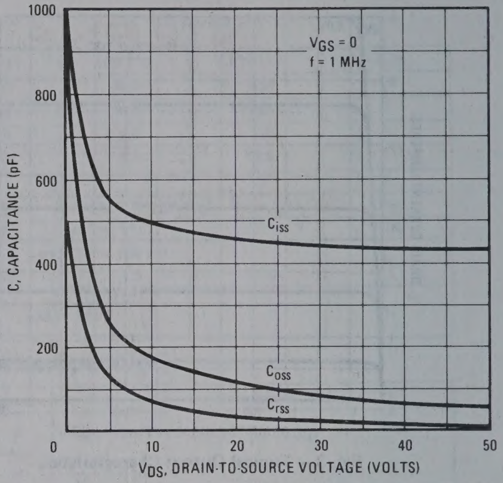


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

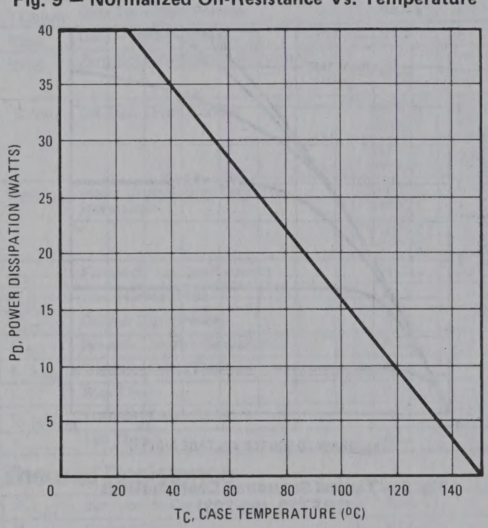


Fig. 11 – Power Vs. Temperature Derating Curve

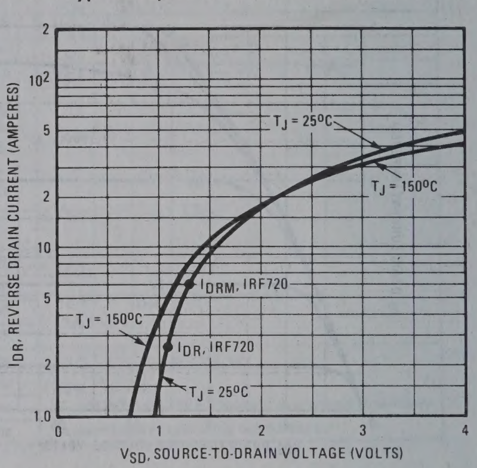


Fig. 12 – Maximum Body-Drain Diode Forward Voltage

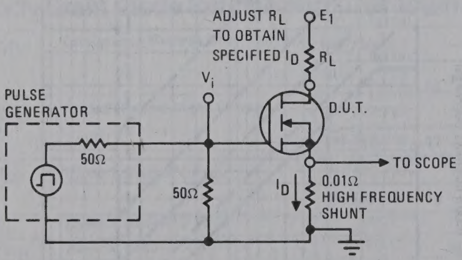
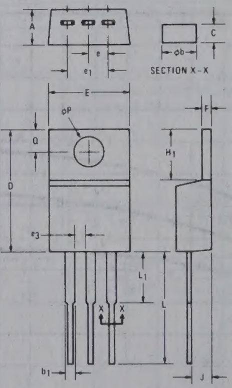


Fig. 13 – Switching Time Test Circuit

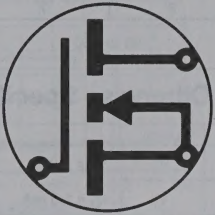


Dimension Table, Case Style TO-220AB

Symbol	Dimensions					
	Inches			Millimeters		
	Min.	Max.	Typ.	Min.	Max.	Typ.
A	0.140	0.190	0.175	3.56	4.82	4.45
b_1	0.045	0.070	0.050	1.15	1.77	1.27
ϕb	0.020	0.045	0.032	0.51	1.14	0.81
C	0.012	0.045	0.018	0.31	1.14	0.46
D	0.560	0.650	0.590	14.23	16.51	14.99
E	0.380	0.420	0.400	9.66	10.66	10.16
e	0.090	0.110	0.100	2.29	2.79	2.54
e_1	0.190	0.210	0.200	4.83	5.33	5.08
e_3	0.045	–	0.050	1.15	–	1.27
F	0.020	0.055	0.050	0.51	1.39	1.27
H_1	0.230	0.270	0.248	5.85	6.85	6.30
J	0.080	0.115	0.105	2.04	2.92	2.67
L	0.500	0.580	0.550	12.70	14.73	13.98
L_1	–	0.250	0.230	–	6.35	5.84
ϕP	0.139	0.161	0.145	3.54	4.08	3.68
Q	0.100	0.135	0.108	2.54	3.42	2.74

INTERNATIONAL RECTIFIER **IOR**

MOFSET TRANSISTORS IRF730 IRF731 IRF732 IRF733



N Channel

400 Volt, 1.0 Ohm HEXFET™ TO-220AB Plastic Package

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

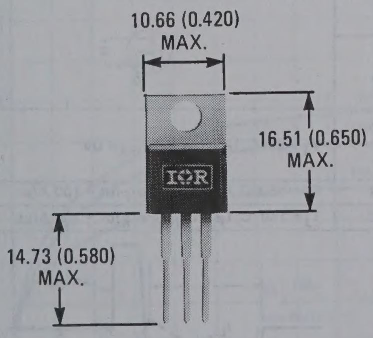
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

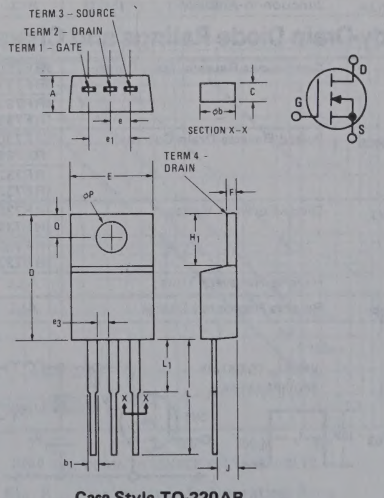
Product Summary

Part Number	V_{DS}	R_{D} (on)	I_D
IRF730	400V	1.0Ω	3.5
IRF731	350V	1.0Ω	3.5
IRF732	400V	1.5Ω	3.0
IRF733	350V	1.5Ω	3.0

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB

Refer to page 190 for Case Style Dimension Table.

IRF730, IRF731, IRF732
IRF733 Devices

Absolute Maximum Ratings

	Parameter	IRF730	IRF731	IRF732	IRF733	Units
V_{DS}	Drain — Source Voltage	400	350	400	350	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	400	350	400	350	V
I_D @ $T_C \cong 102^oC$	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current	8	8	7	7	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	75 (See Fig. 11)				W
	Linear Derating Factor	0.6 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 8	8	7	7	A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC

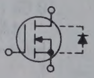
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF730 IRF732	400	–	–	V	V_{GS} = 0
		IRF731 IRF733	350	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSS}	Gate — Body Leakage	ALL	–	–	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_J = 125°C
I_D (on)	On-State Drain Current	IRF730 IRF731	6.0	–	–	A	V_{DS} = 25V, V_{GS} = 10V
		IRF732 IRF733	5.0	–	–	A	
R_{DS} (on)	Static Drain-Source On State Resistance	IRF730 IRF731	–	0.8	1.0	Ω	V_{GS} = 10V, I_D = 2.0A
		IRF732 IRF733	–	1.0	1.5	Ω	
g_{fs}	Forward Transconductance	ALL	2.0	3.5	–	S (℧)	V_{DS} = 100V, I_D = 2A
C_{iss}	Input Capacitance	ALL	–	700	900	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
t_d (on)	Turn-On Delay Time	ALL	–	30	50	ns	V_{DS} = 25V, I_D = 2A (See Fig. 13) T_J = 125°C (MOSFET Switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	50	100	ns	
t_d (off)	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	50	100	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	–	1.0	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF730 IRF731	–	–	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF732 IRF733	–	–	3.0		
I_{DRM}	Pulsed Reverse Drain Current	IRF730 IRF731	–	–	8.0	A	
		IRF732 IRF733	–	–	7.0		
V_{SD}	Diode Forward Voltage	IRF730 IRF731	–	–	1.15	V	T_J = 25°C, I_F = I_{DRM}, V_{GS} = 0V
		IRF732 IRF733	–	–	1.13	V	
t_{rr}	Reverse Recovery Time	ALL	–	550	–	ns	T_J = 150°C, I_F = I_{DRM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	8.0	–	μC	T_J = 150°C, I_F = I_{DRM}, dI_F/dt = 100 A/μs

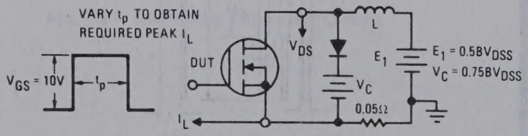


Fig. 1 — Clamped Inductive Test Circuit

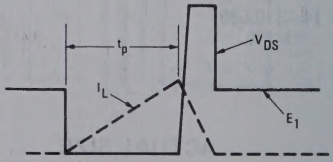


Fig. 2 — Clamped Inductive Waveforms

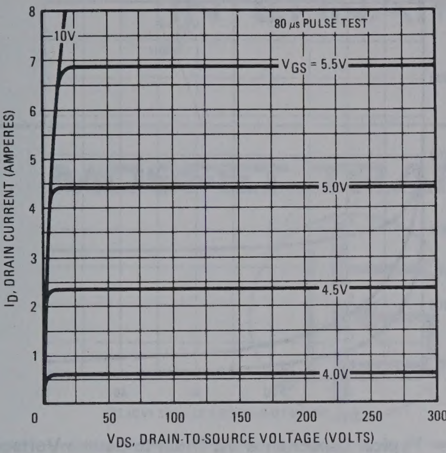


Fig. 3 — Typical Output Characteristics

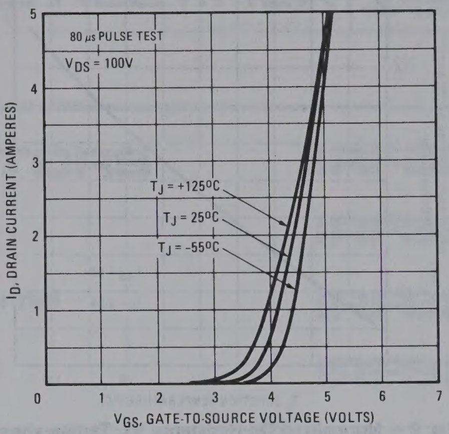


Fig. 4 — Typical Transfer Characteristics

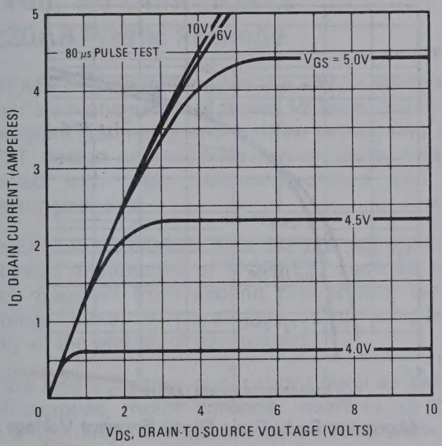


Fig. 5 — Typical Saturation Characteristics (IRF730, IRF731)

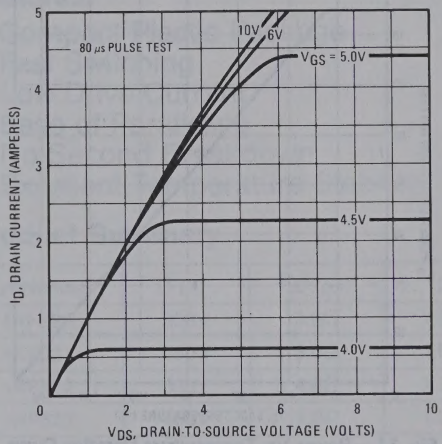


Fig. 6 — Typical Saturation Characteristics (IRF732, IRF733)

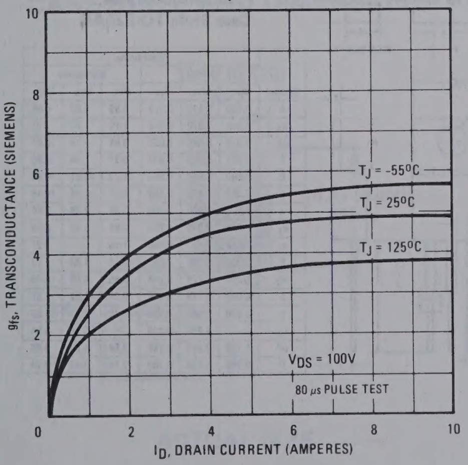


Fig 7. — Typical Transconductance Vs. Drain Current

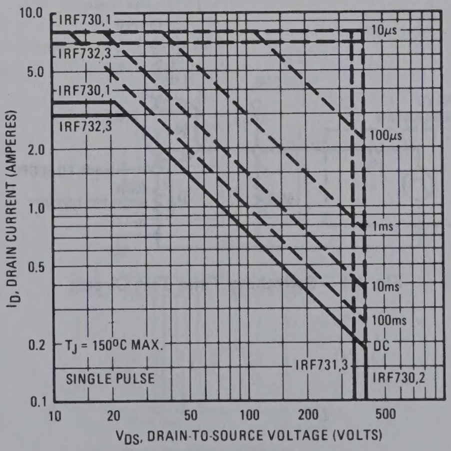


Fig. 8 — Maximum Safe Operating Area

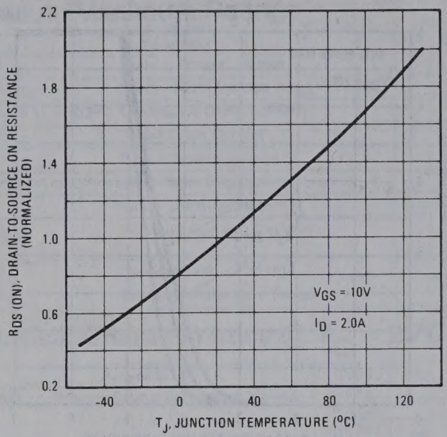


Fig. 9 — Normalized On-Resistance Vs. Temperature

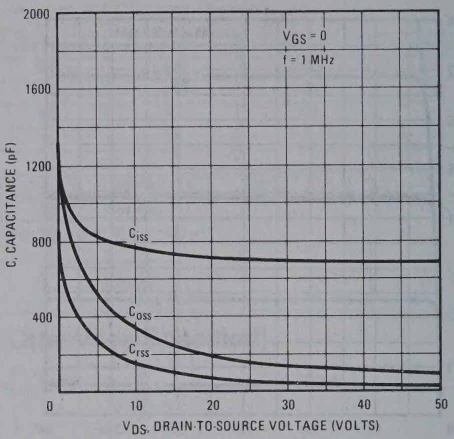


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

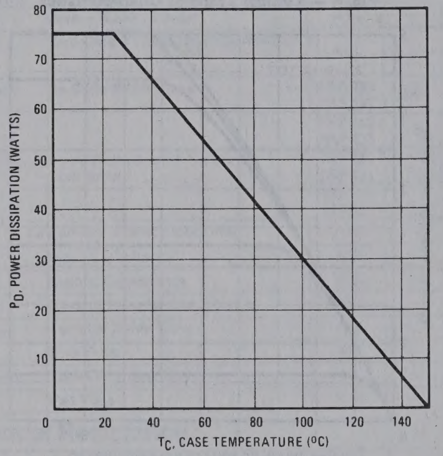


Fig. 11 — Power Vs. Temperature Derating Curve

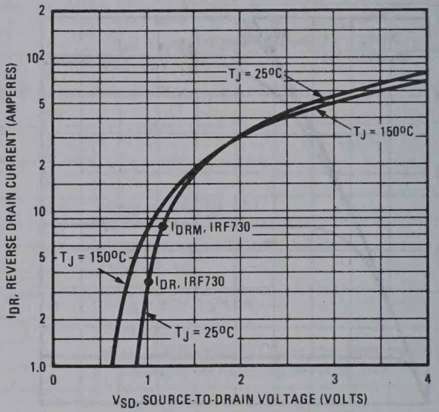


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

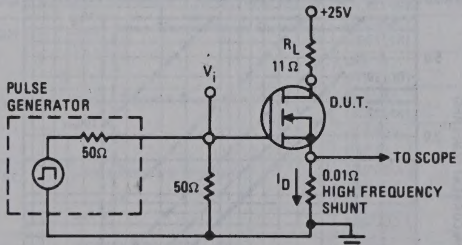
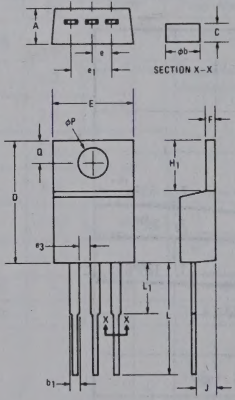


Fig. 13 — Switching Time Test Circuit



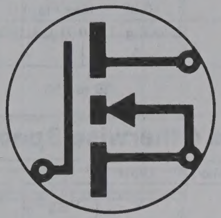
Dimension Table,
Case Style TO-220AB

Symbol	Dimensions					
	Inches			Millimeters		
	Min.	Max.	Typ.	Min.	Max.	Typ.
A	0.140	0.190	0.175	3.56	4.82	4.45
b_1	0.045	0.070	0.050	1.15	1.77	1.27
φb	0.020	0.045	0.032	0.51	1.14	0.81
C	0.012	0.045	0.018	0.31	1.14	0.46
D	0.560	0.650	0.590	14.23	16.51	14.99
E	0.380	0.420	0.400	9.66	10.66	10.16
e	0.090	0.110	0.100	2.29	2.79	2.54
e_1	0.190	0.210	0.200	4.83	5.33	5.08
e_3	0.045	–	0.050	1.15	–	1.27
F	0.020	0.055	0.050	0.51	1.39	1.27
H_1	0.230	0.270	0.248	5.85	6.85	6.30
J	0.080	0.115	0.105	2.04	2.92	2.67
L	0.500	0.580	0.550	12.70	14.73	13.98
L_1	–	0.250	0.230	–	6.35	5.84
φP	0.139	0.161	0.145	3.54	4.08	3.68
Q	0.100	0.135	0.108	2.54	3.42	2.74

INTERNATIONAL RECTIFIER **IOR**

MOSFET TRANSISTORS

IRF820
IRF821
IRF822
IRF823


N Channel

500 Volt, 3.0 Ohm HEXFET™
TO-220AB Plastic Package

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They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

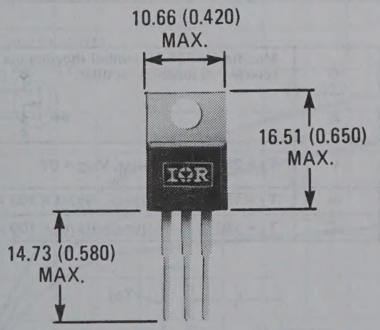
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

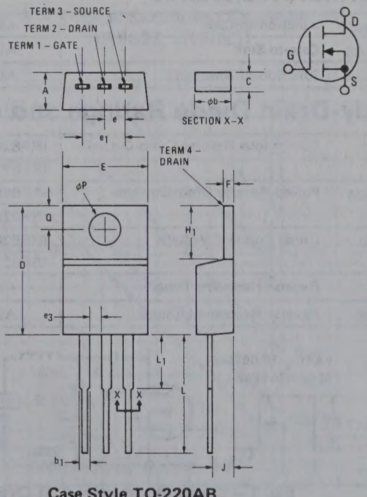
Product Summary

Part Number	V_{DS}	R_{D} (on)	I_{D}
IRF820	500V	3.0Ω	1.5A
IRF821	450V	3.0Ω	1.5A
IRF822	500V	4.0Ω	1.0A
IRF823	450V	4.0Ω	1.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB.

Refer to page 194 for Case Style Dimension Table.

Absolute Maximum Ratings

Parameter		IRF820	IRF821	IRF822	IRF823	Units
V_{DS}	Drain – Source Voltage	500	450	500	450	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	500	450	500	450	V
I_D @ $T_C \cong 96.5^oC$	Continuous Drain Current	1.5	1.5	1	1	A
I_{DM}	Pulsed Drain Current	5	5	4	4	A
V_{GS}	Gate – Source Voltage	±20				V
P_D	Max. Power Dissipation	40 (See Fig. 11)				W
	Linear Derating Factor	0.32 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 5	5	4	4	A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC

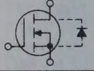
Electrical Characteristics @ $T_C = 25°C$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRF820 IRF822	500	–	–	V	$V_{GS} = 0$
		IRF821 IRF823	450	–	–	V	$I_D = 4.0$ mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate – Body Leakage	ALL	–	–	500	nA	$V_{GS} = 20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0	mA	V_{DS} = 0.8 x Max. Rating, $V_{GS} = 0$
			–	0.2	4.0	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_J = 25^oC$ to 125^oC
$I_{D\ (on)}$	On-State Drain Current	IRF820 IRF821	2.5	–	–	A	$V_{DS} = 25V$, $V_{GS} = 10V$
		IRF822 IRF823	2.0	–	–	A	
$R_{DS\ (on)}$	Static Drain-Source On State Resistance	IRF820 IRF821	–	2.5	3.0	Ω	$V_{GS} = 10V$, $I_D = 1A$
		IRF822 IRF823	–	3.0	4.0	Ω	
g_{fs}	Forward Transconductance	ALL	1.0	1.75	–	S (℧)	$V_{DS} = 100V$, $I_D = 1A$
C_{iss}	Input Capacitance	ALL	–	300	400	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	–	75	150	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	30	60	ns	$I_D = 1A$, $E_1 = 0.5\ BV_{DSS}$ (See Fig. 13)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	30	60	ns	$T_J = 125^oC$ (MOSFET Switching times are essentially independent of operating temperature.)
t_f	Fall Time	ALL	–	15	30	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	–	1.0	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF820, 821	–	–	1.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF822, 823	–	–	1.0		
I_{DRM}	Pulsed Reverse Drain Current	IRF820, 821	–	–	5.0	A	
		IRF822, 823	–	–	4.0		
V_{SD}	Diode Forward Voltage	IRF820, 821	–	–	1.0	V	$T_J = 25^oC$, $I_F = I_{DRM}$, $V_{GS} = 0V$
		IRF822, 823	–	–	0.9		
t_{rr}	Reverse Recovery Time	ALL	–	200	–	ns	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.0	–	μC	$T_J = 150^oC$, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

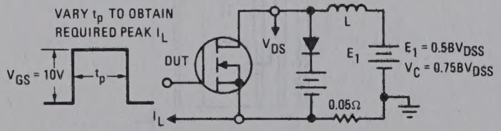


Fig. 1 – Clamped Inductive Test Circuit

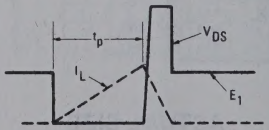


Fig. 2 – Clamped Inductive Waveforms

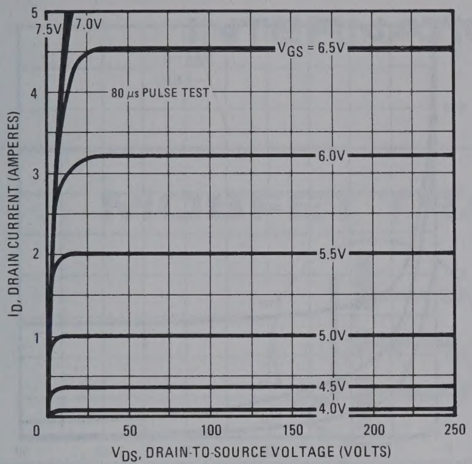


Fig. 3 — Typical Output Characteristics

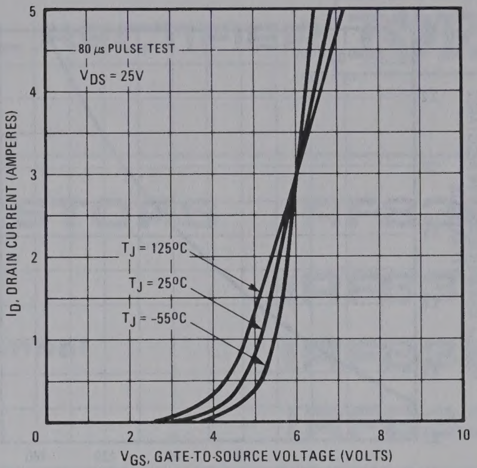


Fig. 4 — Typical Transfer Characteristics

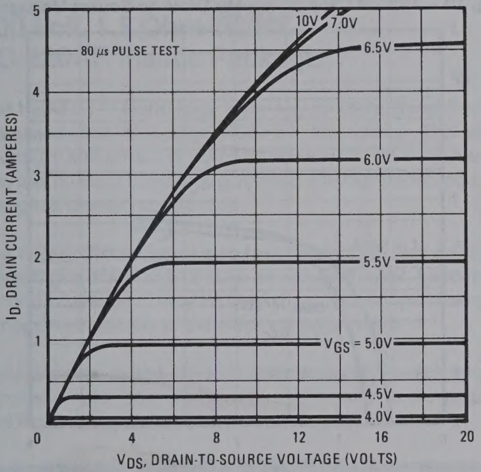


Fig. 5 — Typical Saturation Characteristics (IRF820, IRF821)

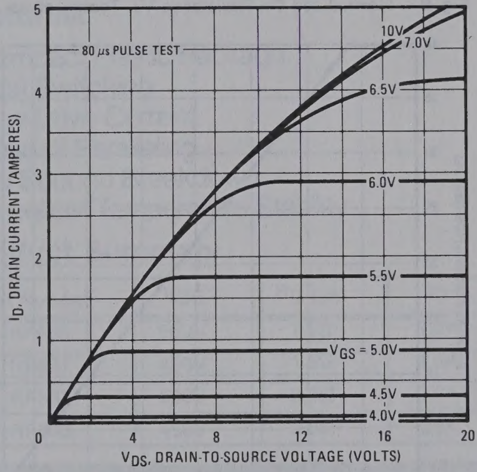


Fig. 6 — Typical Saturation Characteristics (IRF822, IRF823)

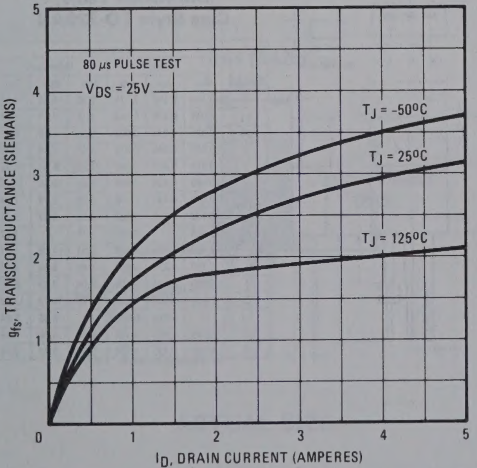


Fig. 7 — Typical Transconductance Vs. Drain Current

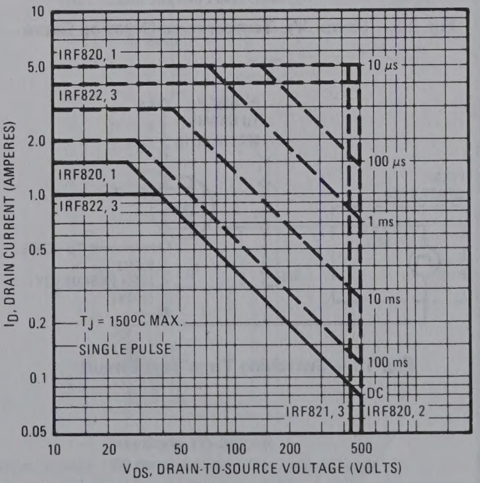


Fig. 8 — Maximum Safe Operating Area

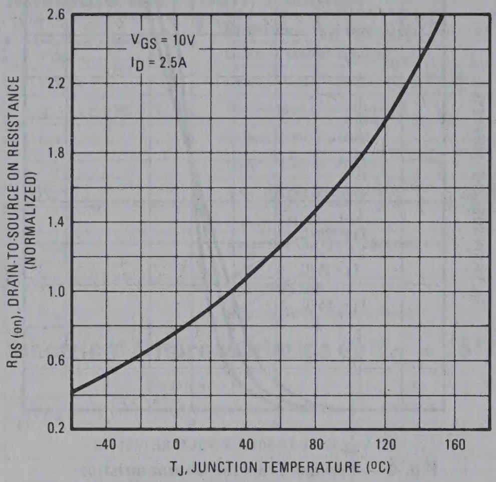


Fig. 9 — Normalized On-Resistance Vs. Temperature

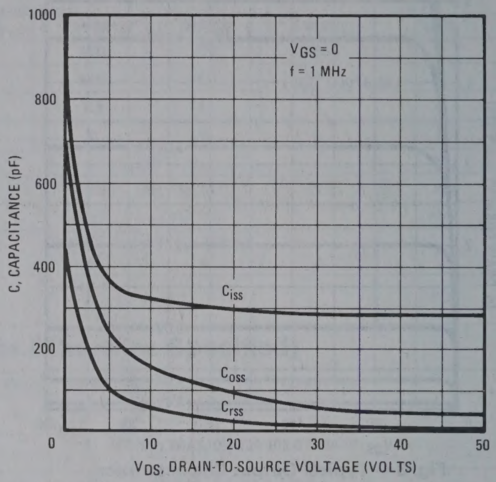


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

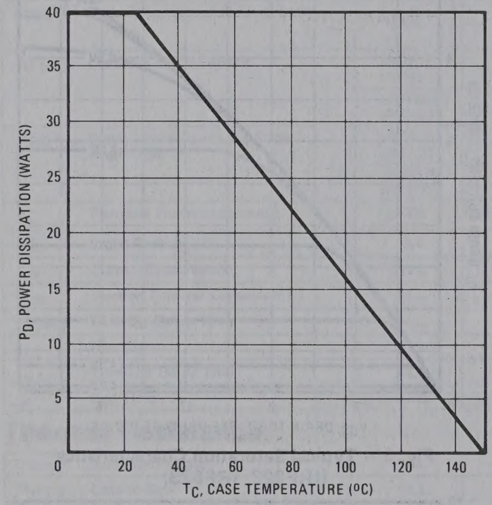


Fig. 11 — Power Vs. Temperature Derating Curve

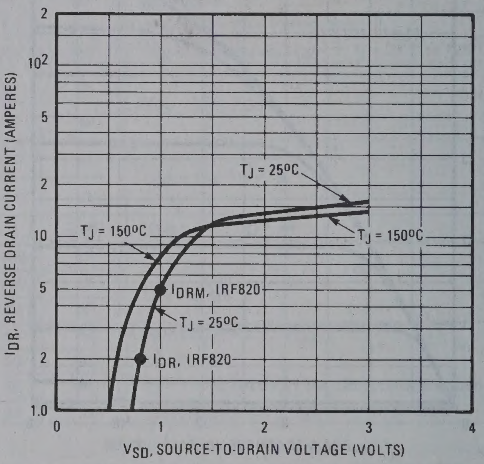


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

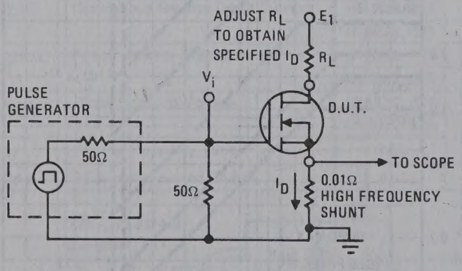
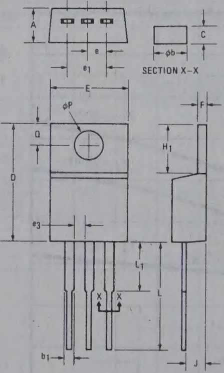


Fig. 13 — Switching Time Test Circuit

Dimension Table, Case Style TO-220AB

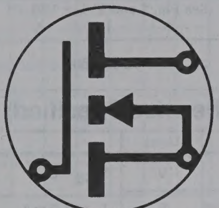


Symbol	Dimensions					
	Inches			Millimeters		
	Min.	Max.	Typ.	Min.	Max.	Typ.
A	0.140	0.190	0.175	3.56	4.82	4.45
b_1	0.045	0.070	0.050	1.15	1.77	1.27
φb	0.020	0.045	0.032	0.51	1.14	0.81
C	0.012	0.045	0.018	0.31	1.14	0.46
D	0.560	0.650	0.590	14.23	16.51	14.99
E	0.380	0.420	0.400	9.66	10.66	10.16
e	0.090	0.110	0.100	2.29	2.79	2.54
e_1	0.190	0.210	0.200	4.83	5.33	5.08
e_3	0.045	–	0.050	1.15	–	1.27
F	0.020	0.055	0.050	0.51	1.39	1.27
H_1	0.230	0.270	0.248	5.85	6.85	6.30
J	0.080	0.115	0.105	2.04	2.92	2.67
L	0.500	0.580	0.550	12.70	14.73	13.98
L_1	–	0.250	0.230	–	6.35	5.84
φP	0.139	0.161	0.145	3.54	4.08	3.68
Q	0.100	0.135	0.108	2.54	3.42	2.74

PD-9.311

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF830 IRF831 IRF832 IRF833



500 Volt, 1.5 Ohm HEXFET™ TO-220AB Plastic Package

The HEXFET^{TM} technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

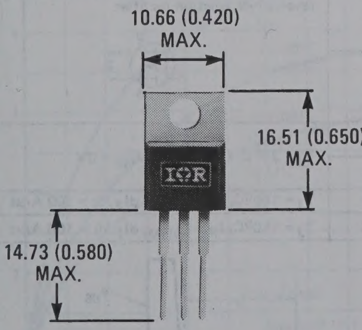
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

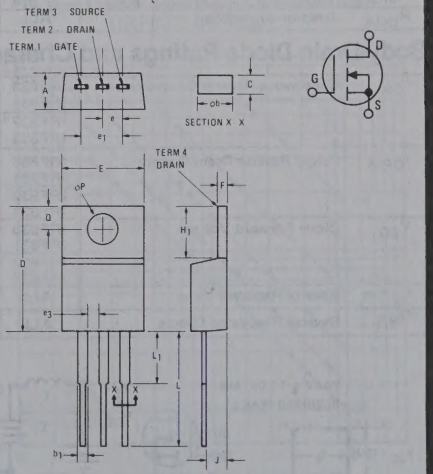
Product Summary

Part Number	V_{DS}	R_{D} (on)	I_D
IRF830	500V	1.5Ω	3.0A
IRF831	450V	1.5Ω	3.0A
IRF832	500V	2.0Ω	2.5A
IRF833	450V	2.0Ω	2.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB

Refer to page 198 for Case Style Dimension Table.

IRF830, IRF831, IRF832, IRF833 Devices

Absolute Maximum Ratings

Parameter		IRF830	IRF831	IRF832	IRF833	Units
V_{DS}	Drain — Source Voltage	500	450	500	450	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	500	450	500	450	V
I_D @ $T_C \cong 102^oC$	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current	7.0	7.0	6.0	6.0	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	75 (See Fig. 11)				W
	Linear Derating Factor	0.6 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 7	7	6	6	A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC

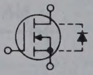
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF830 IRF832	500	—	—	V	V_{GS} = 0 I_D = 4.0 mA
		IRF831 IRF833	450	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	0.1	1.0	mA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0
			—	0.2	4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_J = 25°C to 125°C
I_D (on)	On-State Drain Current	IRF830 IRF831	5.0	—	—	A	V_{DS} = 25V, V_{GS} = 10V
		IRF832 IRF833	4.0	—	—	A	
R_{DS} (on)	Static Drain-Source On State Resistance	IRF830 IRF831	—	1.3	1.5	Ω	V_{GS} = 10V, I_D = 1.5A
		IRF832 IRF833	—	1.5	2.0	Ω	
g_{fs}	Forward Transconductance	ALL	1.5	2.5	—	S (℧)	V_{DS} = 100V, I_D = 1.5A
C_{iss}	Input Capacitance	ALL	—	700	900	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL	—	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	30	60	pF	
t_d (on)	Turn-On Delay Time	ALL	—	30	50	ns	I_D = 1.5A, E_1 = 0.5 BV_{DSS} (See Fig. 13) T_J = 125°C (MOSFET Switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	40	80	ns	
t_d (off)	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	40	80	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	1.0	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF830 IRF831	—	—	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF832 IRF833	—	—	2.5		
I_{DRM}	Pulsed Reverse Drain Current	IRF830 IRF831	—	—	7.0	A	
		IRF832 IRF833	—	—	6.0		
V_{SD}	Diode Forward Voltage	IRF830 IRF831	—	—	1.13	V	T_J = 25°C, I_F = I_{DRM}, V_{GS} = 0V
		IRF832 IRF833	—	—	1.10	V	
t_{rr}	Reverse Recovery Time	ALL	—	500	—	ns	T_J = 150°C, I_F = I_{DRM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	7.0	—	μC	T_J = 150°C, I_F = I_{DRM}, dI_F/dt = 100 A/μs

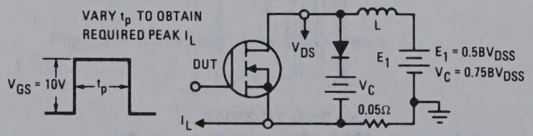


Fig. 1 — Clamped Inductive Test Circuit

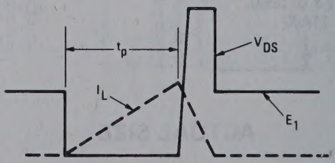


Fig. 2 — Clamped Inductive Waveforms

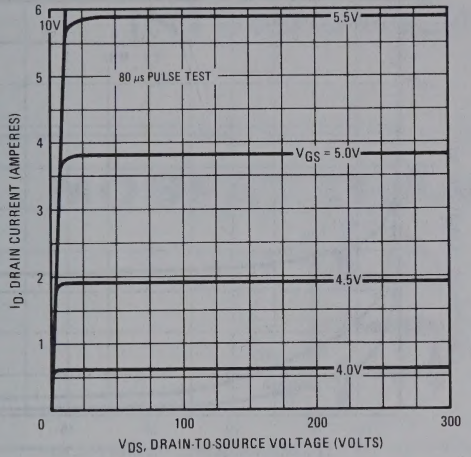


Fig. 3 — Typical Output Characteristics

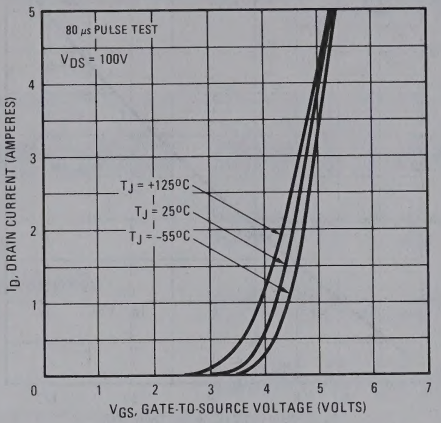


Fig. 4 — Typical Transfer Characteristics

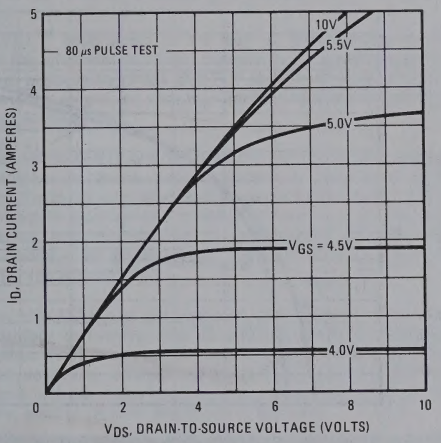


Fig. 5 — Typical Saturation Characteristics (IRF830, IRF831)

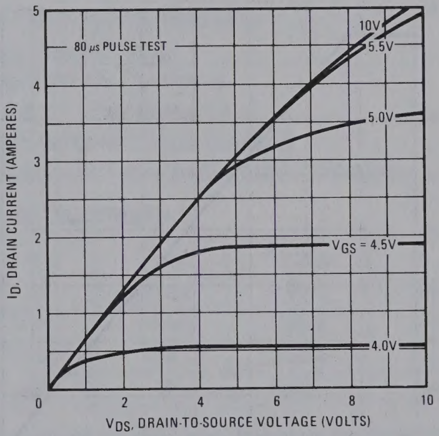


Fig. 6 — Typical Saturation Characteristics (IRF832, IRF833)

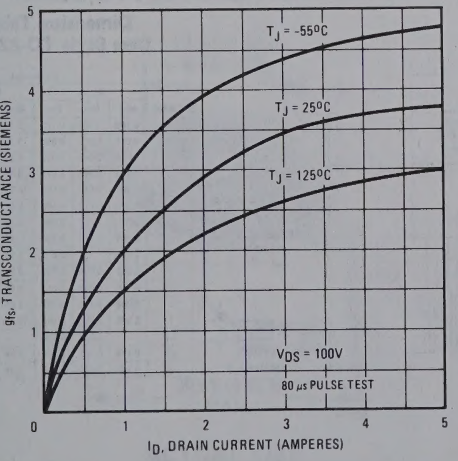


Fig. 7 — Typical Transconductance Vs. Drain Current

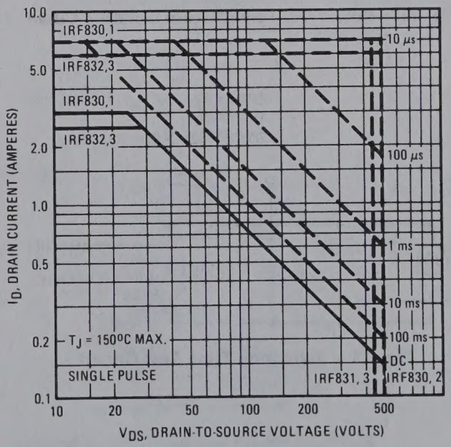


Fig. 8 — Maximum Safe Operating Area

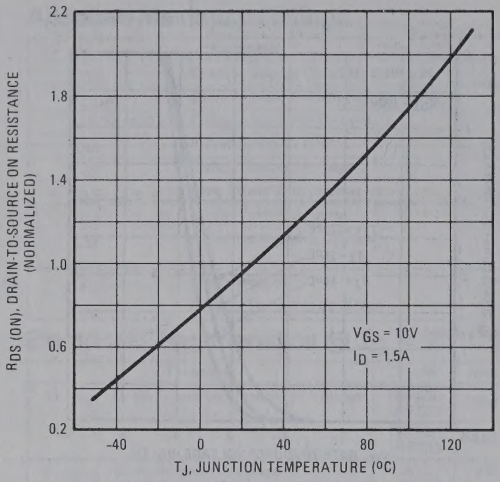


Fig. 9 — Normalized On-Resistance Vs. Temperature

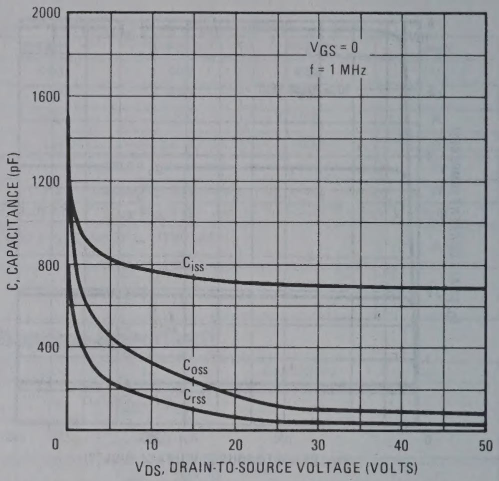


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

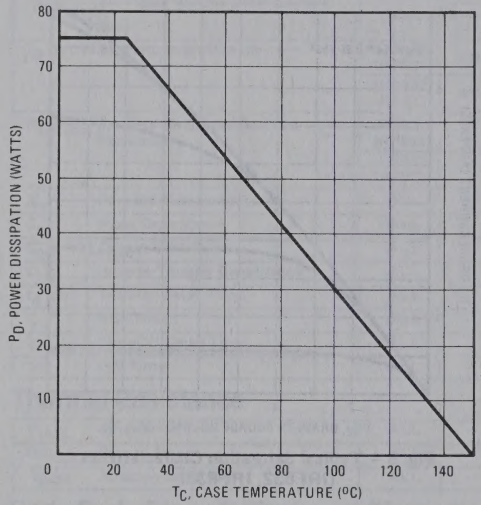


Fig. 11 — Power Vs. Temperature Derating Curve

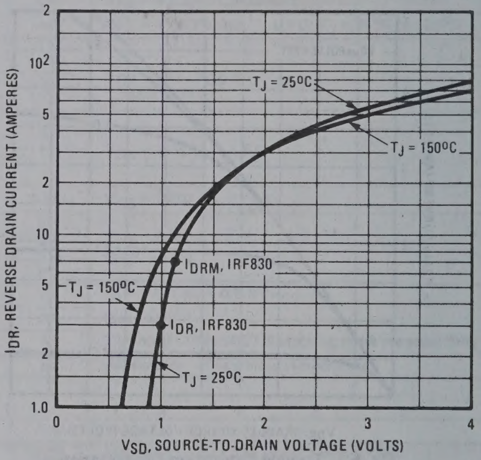


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

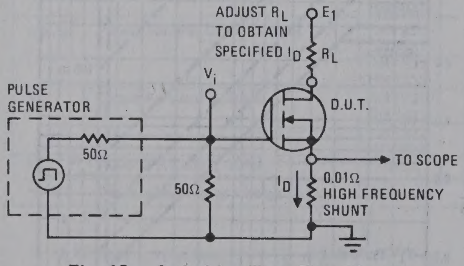
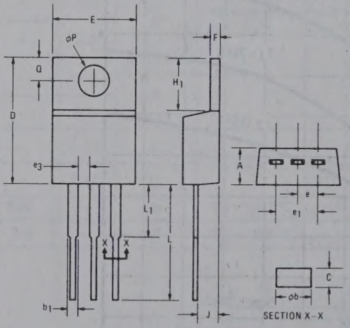


Fig. 13 — Switching Time Test Circuit

Dimension Table, Case Style TO-220AB

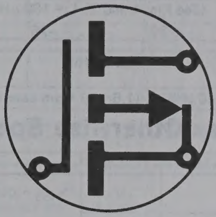


Symbol	Dimensions					
	Inches			Millimeters		
	Min.	Max.	Typ.	Min.	Max.	Typ.
A	0.140	0.190	0.175	3.56	4.82	4.45
b_1	0.045	0.070	0.050	1.15	1.77	1.27
φb	0.020	0.045	0.032	0.51	1.14	0.81
C	0.012	0.045	0.018	0.31	1.14	0.46
D	0.560	0.650	0.590	14.23	16.51	14.99
E	0.380	0.420	0.400	9.66	10.66	10.16
e	0.090	0.110	0.100	2.29	2.79	2.54
e_1	0.190	0.210	0.200	4.83	5.33	5.08
e_3	0.045	–	0.050	1.15	–	1.27
F	0.020	0.055	0.050	0.51	1.39	1.27
H_1	0.230	0.270	0.248	5.85	6.85	6.30
J	0.080	0.115	0.105	2.04	2.92	2.67
L	0.500	0.580	0.550	12.70	14.73	13.98
L_1	–	0.250	0.230	–	6.35	5.84
φP	0.139	0.161	0.145	3.54	4.08	3.68
Q	0.100	0.135	0.108	2.54	3.42	2.74

PD-9.318

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF9130 IRF9131 IRF9132 IRF9133



P Channel

100Volt, 0.30 Ohm HEXFET™

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N channel HEXFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and excellent temperature stability. The P channel IRF9130 device is an approximate electrical complement to the N channel IRF120 HEXFET.

P channel HEXFETs are intended for use in power stages where complementary symmetry with N channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

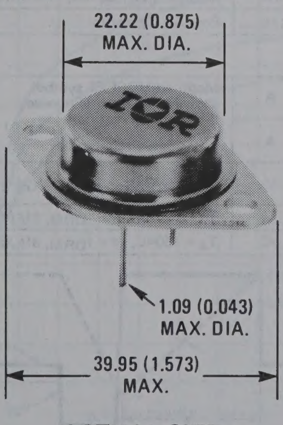
Features:

- P Channel Versatility
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

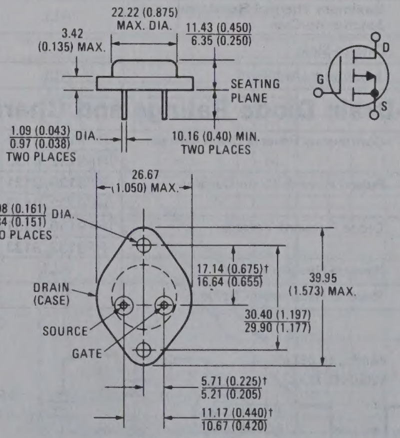
Product Summary

Part Number	V_{DS}	R_D (on)	I_D
IRF9130	-100V	0.30Ω	-8A
IRF9131	-60V	0.30Ω	-8A
IRF9132	-100V	0.40Ω	-7A
IRF9133	-60V	0.40Ω	-7A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings

	Parameter	IRF9130	IRF9131	IRF9132	IRF9133	Units
V_{DS}	Drain – Source Voltage	-100	-60	-100	-60	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	-100	-60	-100	-60	V
I_D @ T_C = 90°C	Continuous Drain Current	-8	-8	-7	-7	A
I_{DM}	Pulsed Drain Current	-30	-30	-25	-25	A
V_{GS}	Gate – Source Voltage	±20				V
P_D	Max. Power Dissipation	75 (See Fig. 11)				W
	Linear Derating Factor	0.6 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH -30	-30	-25	-25	A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10 s)				°C

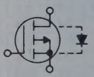
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRF9130 IRF9132	-100	–	–	V	V_{GS} = 0V
		IRF9131 IRF9133	-60	–	–	V	I_D = -1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	–	-4.0	V	V_{DS} = V_{GS}, I_D = -1.0 mA
I_{GSS}	Gate – Body Leakage	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	-0.1	-1.0	mA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	-0.2	-4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0V, T_J = 125°C
$I_{D\ (on)}$	On-State Drain Current	IRF9130 IRF9131	-12	–	–	A	V_{DS} = -25V, V_{GS} = -10V
		IRF9132 IRF9133	-10	–	–	A	
$R_{DS\ (on)}$	Static Drain-Source On State Resistance	IRF9130 IRF9131	–	0.25	0.30	Ω	V_{GS} = -10V, I_D -4A
		IRF9132 IRF9133	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance	ALL	2.0	3.5	–	S (℧)	V_{DS} = -25V, I_D = -4A
C_{iss}	Input Capacitance	ALL	–	500	700	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	200	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	30	60	ns	I_D = -4A, E_1 = 0.5 BV_{DSS} (See Fig. 13)
t_r	Rise Time	ALL	–	70	140	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	70	140	ns	T_J = 125°C (MOSFET switching times are essentially independent of operating temperature.
t_f	Fall Time	ALL	–	70	140	ns	

Thermal Resistance

R_{thJC}	Maximum Thermal Resistance Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	–	0.2	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF9130, 9131	–	–	-8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF9132, 9133	–	–	-7.0		
I_{DRM}	Pulsed Reverse Drain Current	IRF9130, 9131	–	–	-30	A	
		IRF9132, 9133	–	–	-25		
V_{SD}	Diode Forward Voltage	IRF9130, 9131	–	–	-5.5	V	T_J = 25°C, I_F = I_{DRM}, V_{GS} = 0V
		IRF9132, 9133	–	–	-5.3		
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, I_F = I_{DRM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = I_{DRM}, dI_F/dt = 100 A/μs

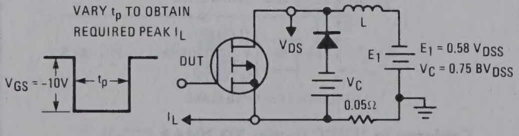


Fig. 1 – Clamped Inductive Test Circuit

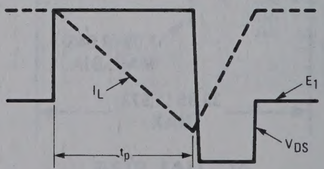


Fig. 2 – Clamped Inductive Waveforms

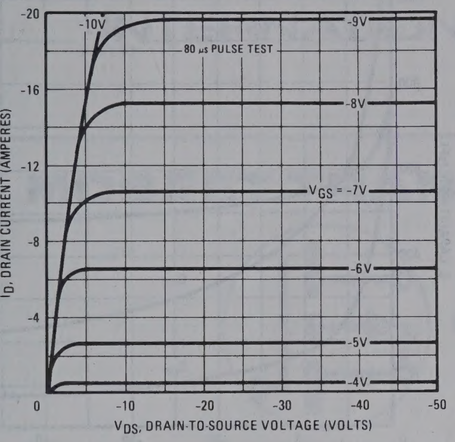


Fig. 3 — Typical Output Characteristics

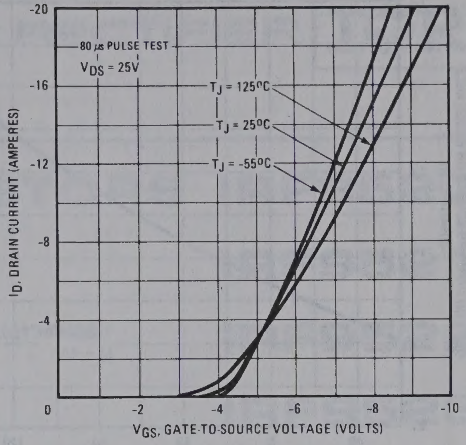


Fig. 4 — Typical Transfer Characteristics

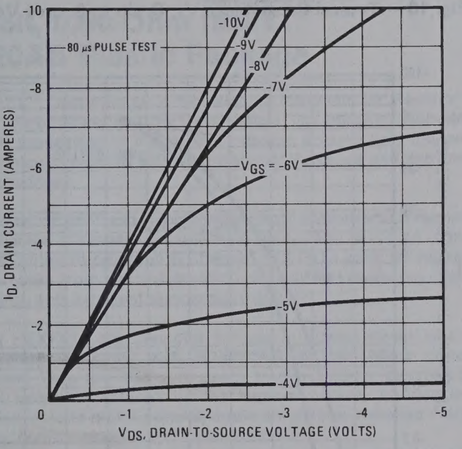


Fig. 5 — Typical Saturation Characteristics (IRF9130, IRF9131)

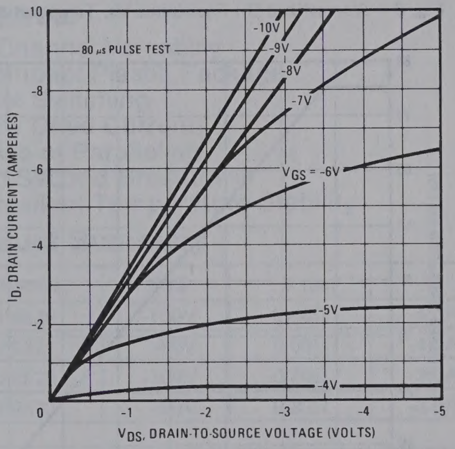


Fig. 6 — Typical Saturation Characteristics (IRF9132, IRF9133)

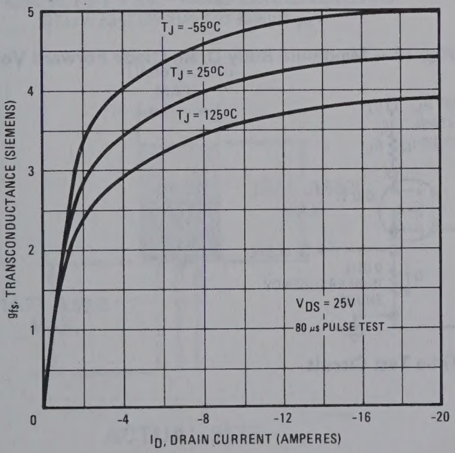


Fig. 7 — Typical Transconductance Vs. Drain Current

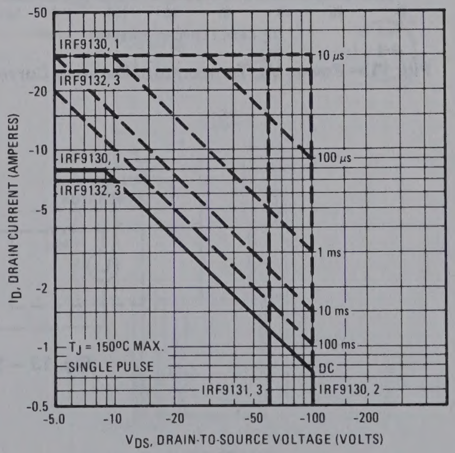


Fig. 8 — Maximum Safe Operating Area

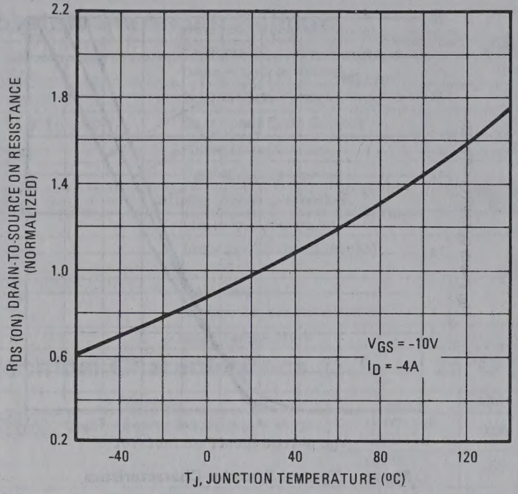


Fig. 9 — Normalized On-Resistance Vs. Temperature

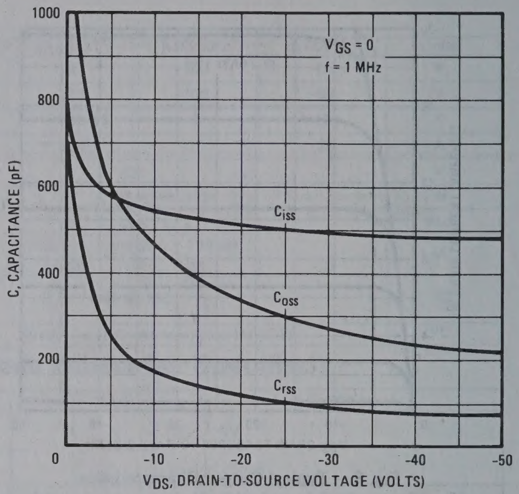


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

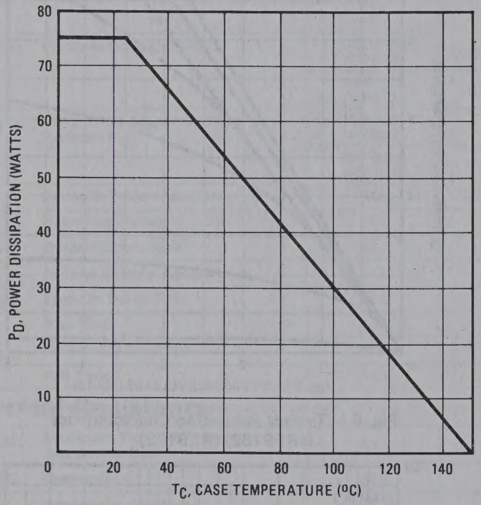


Fig. 11 — Power Vs. Temperature Derating Curve

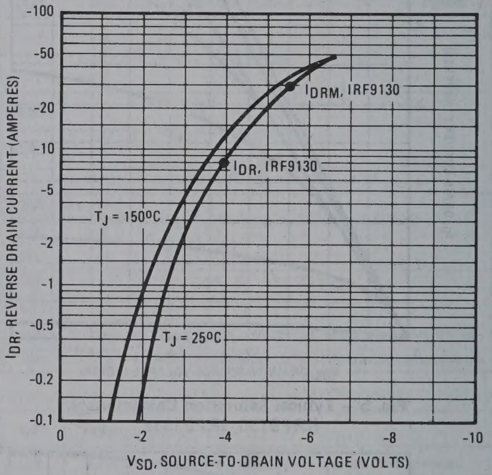


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

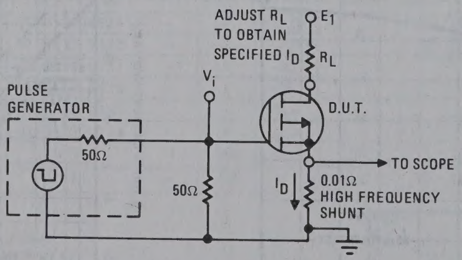
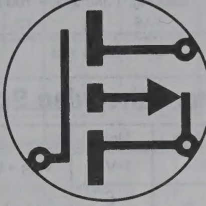


Fig. 13 — Switching Time Test Circuit

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF9520 IRF9521 IRF9522 IRF9523



P Channel

100 Volt, 0.60 Ohm HEXFET™ TO-220AB Plastic Package

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N channel HEXFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and excellent temperature stability.

P channel HEXFETs are intended for use in power stages where complementary symmetry with N channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

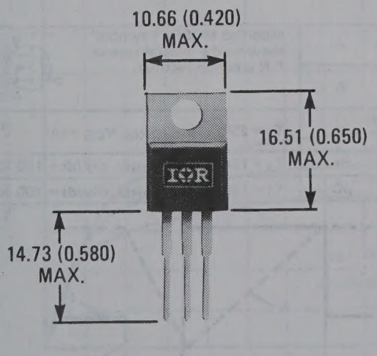
Features:

- P Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

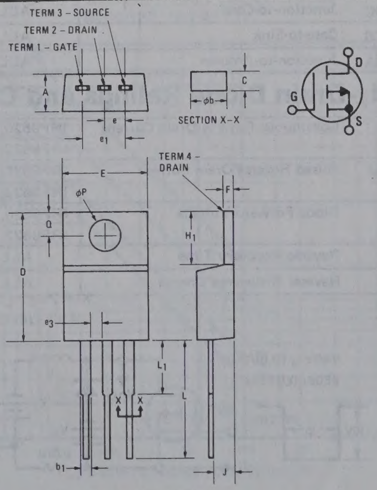
Product Summary

Part Number	V_{DS}	R_D (on)	I_D
IRF9520	-100V	0.60Ω	-4.0A
IRF9521	-60V	0.60Ω	-4.0A
IRF9522	-100V	0.80Ω	-3.5A
IRF9523	-60V	0.80Ω	-3.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB

Refer to page 206 for Case Style Dimension Table.

Absolute Maximum Ratings

	Parameter	IRF9520	IRF9521	IRF9522	IRF9523	Units
V_{DS}	Drain — Source Voltage	-100	-60	-100	-60	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	-100	-60	-100	-60	V
I_D @ $T_C \cong 100^oC$	Continuous Drain Current	-4.0	-4.0	-3.5	-3.5	A
I_{DM}	Pulsed Drain Current	-15	-15	-12	-12	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	40 (See Fig. 11)				W
	Linear Derating Factor	0.32 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH -15	-15	-12	-12	A
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				^oC

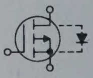
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF9520 IRF9522	-100	—	—	V	V_{GS} = 0V
		IRF9521 IRF9523	-60	—	—	V	I_D = -1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -1.0 mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	-0.1	-1.0	mA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	-0.2	-4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0V, T_J = 125°C
$I_{D\ (on)}$	On-State Drain Current	IRF9520 IRF9521	-6.0	—	—	A	V_{DS} = -25V, V_{GS} = -10V
		IRF9522 IRF9523	-5.0	—	—	A	
$R_{DS\ (on)}$	Static Drain-Source On State Resistance	IRF9520 IRF9521	—	0.5	0.6	Ω	V_{GS} = -10V, I_D = -2A
		IRF9522 IRF9523	—	0.6	0.8	Ω	
g_{fs}	Forward Transconductance	ALL	0.9	1.8	—	S (℧)	V_{DS} = -25V, I_D = -2A
C_{iss}	Input Capacitance	ALL	—	300	450	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	200	350	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	50	100	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	—	25	50	ns	I_D -2A, E_1 = 0.5 BV_{DSS} (See Fig. 13) T_J = 125°C (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	50	100	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	50	100	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	1.0	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF9520, 9521	—	—	-4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF9522, 9523	—	—	-3.5		
I_{DRM}	Pulsed Reverse Drain Current	IRF9520, 9521	—	—	-15	A	
		IRF9522, 9523	—	—	-12		
V_{SD}	Diode Forward Voltage	IRF9520, 9521	—	—	-5.5	V	T_J = 25°C, I_F = I_{DRM}, V_{GS} = 0V
		IRF9522, 9523	—	—	-5.2		
t_{rr}	Reverse Recovery Time	ALL	—	150	—	ns	T_J = 150°C, I_F = I_{DRM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.0	—	μC	T_J = 150°C, I_F = I_{DRM}, dI_F/dt = 100 A/μs

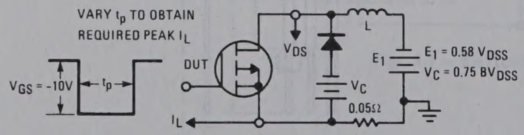


Fig. 1 — Clamped Inductive Test Circuit

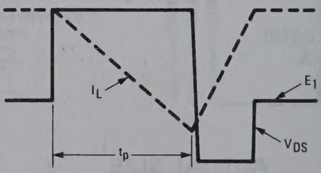


Fig. 2 — Clamped Inductive Waveform

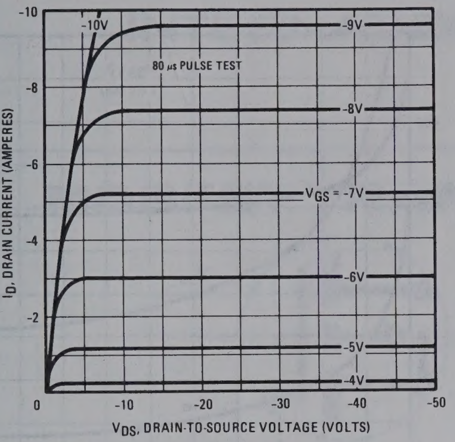


Fig. 3 — Typical Output Characteristics

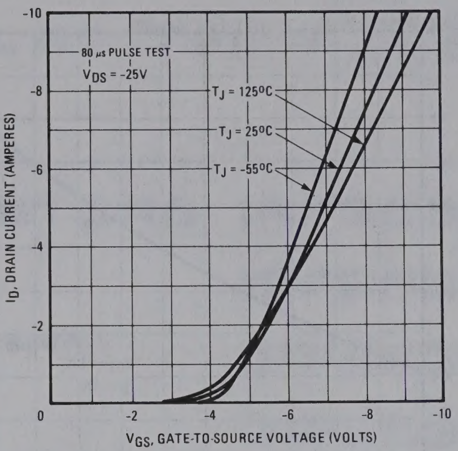


Fig. 4 — Typical Transfer Characteristics

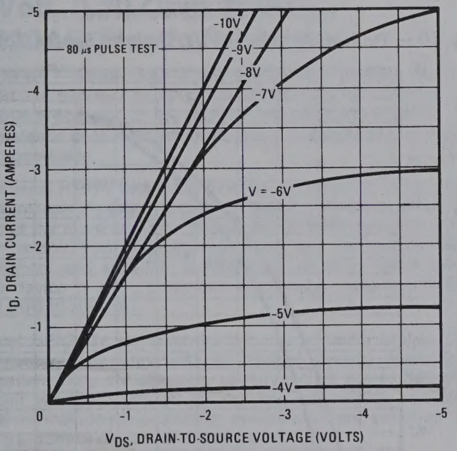


Fig. 5 — Typical Saturation Characteristics (IRF9520, IRF9521)

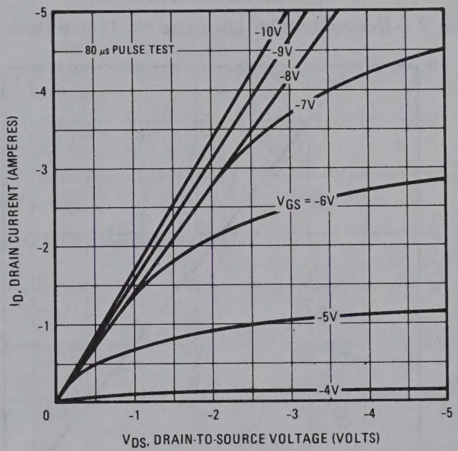


Fig. 6 — Typical Saturation Characteristics (IRF9522, IRF9523)

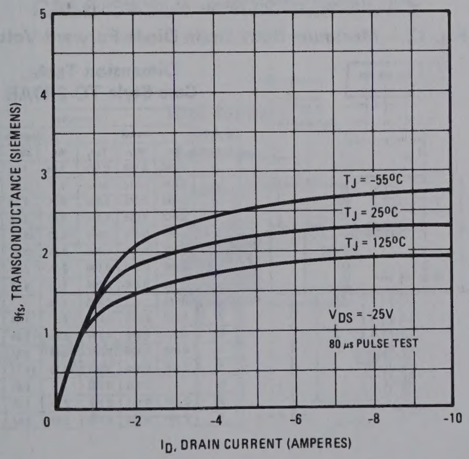


Fig. 7 — Typical Transconductance Vs. Drain Current

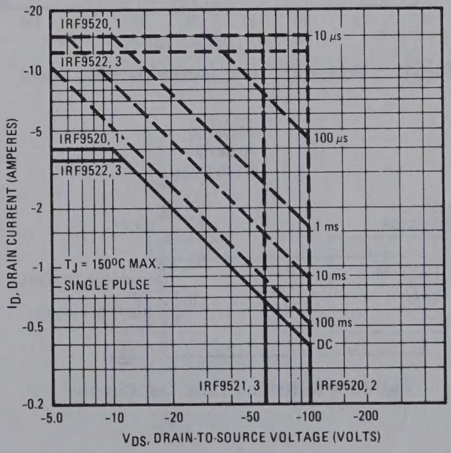


Fig. 8 — Maximum Safe Operating Area

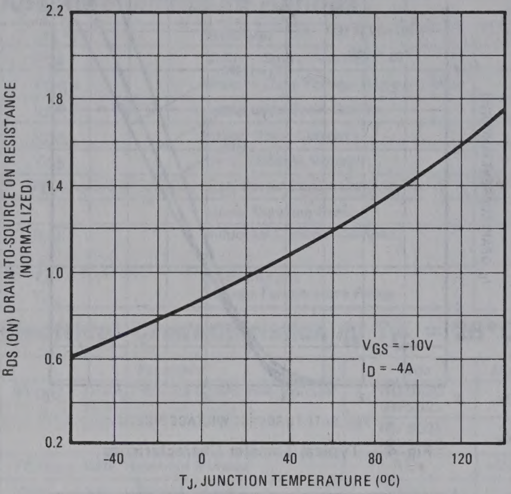


Fig. 9 — Normalized On-Resistance Vs. Temperature

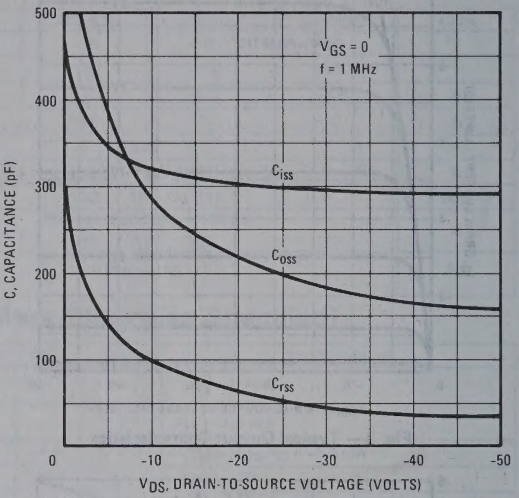


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

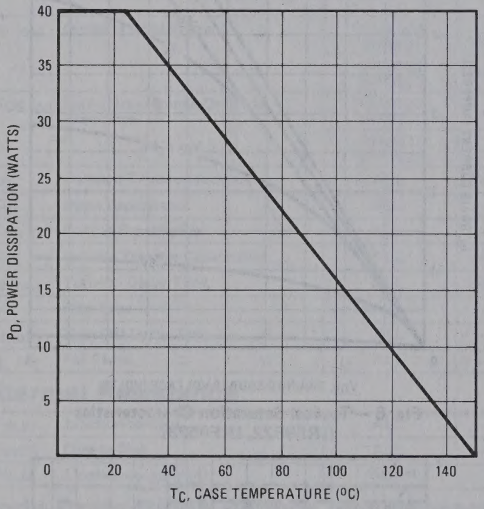


Fig. 11 — Power Vs. Temperature Derating Curve

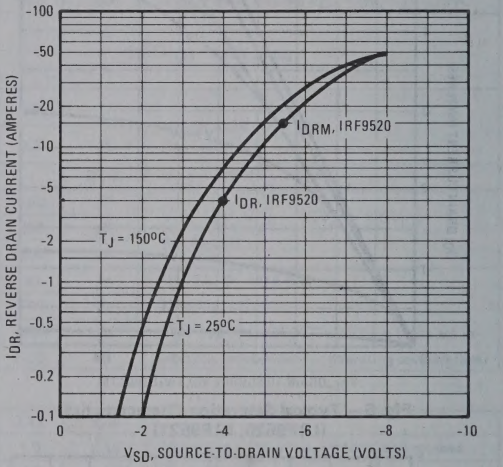


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

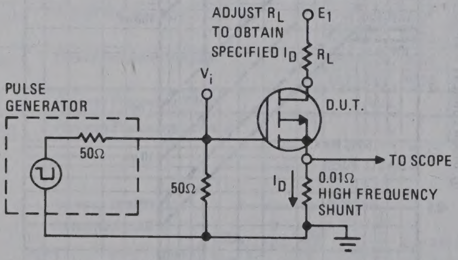
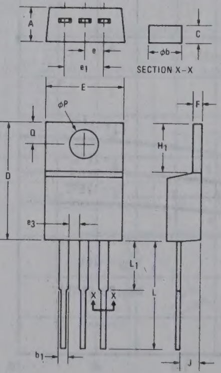

ADJUST R_L TO OBTAIN SPECIFIED I_D
E_1
R_L
V_i
D.U.T.
PULSE GENERATOR
50Ω
50Ω
TO SCOPE
I_D
0.01Ω HIGH FREQUENCY SHUNT

Fig. 13 — Switching Time Test Circuit

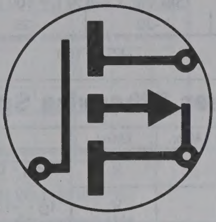


Dimension Table, Case Style TO-220AB

Symbol	Dimensions					
	Inches			Millimeters		
	Min.	Max.	Typ.	Min.	Max.	Typ.
A	0.140	0.190	0.175	3.56	4.82	4.45
b_1	0.045	0.070	0.050	1.15	1.77	1.27
ϕb	0.020	0.045	0.032	0.51	1.14	0.81
C	0.012	0.045	0.018	0.31	1.14	0.46
D	0.560	0.650	0.590	14.23	16.51	14.99
E	0.380	0.420	0.400	9.66	10.66	10.16
e	0.090	0.110	0.100	2.29	2.79	2.54
e_1	0.190	0.210	0.200	4.83	5.33	5.08
e_3	0.045	–	0.050	1.15	–	1.27
F	0.020	0.055	0.050	0.51	1.39	1.27
H_1	0.230	0.270	0.248	5.85	6.85	6.30
J	0.080	0.115	0.105	2.04	2.92	2.67
L	0.500	0.580	0.550	12.70	14.73	13.98
L_1	–	0.250	0.230	–	6.35	5.84
ϕP	0.139	0.161	0.145	3.54	4.08	3.68
Q	0.100	0.135	0.108	2.54	3.42	2.74

INTERNATIONAL RECTIFIER IOR

MOSFET TRANSISTORS IRF9530 IRF9531 IRF9532 IRF9533



P Channel

100 Volt, 0.30 Ohm HEXFET™ TO-220AB Plastic Package

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N channel HEXFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and excellent temperature stability. The P channel IRF9530 device is an approximate electrical complement to the N channel IRF520 HEXFET.

P channel HEXFETs are intended for use in power stages where complementary symmetry with N channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

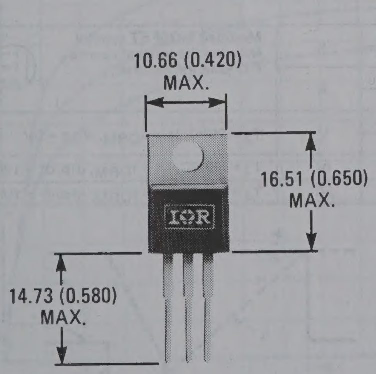
Features:

- P Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

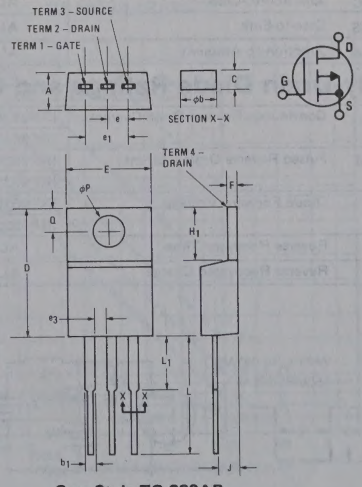
Product Summary

Part Number	V_{DS}	R_{D} (on)	I_D
IRF9530	-100V	0.30Ω	-7A
IRF9531	-60V	0.30Ω	-7A
IRF9532	-100V	0.40Ω	-6A
IRF9533	-60V	0.40Ω	-6A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB

Refer to page 210 for Case Style Dimension Table.

IRF9530, IRF9531, IRF9532, IRF9533 Devices

Absolute Maximum Ratings

	Parameter	IRF9530	IRF9531	IRF9532	IRF9533	Units
V_{DS}	Drain — Source Voltage	−100	−60	−100	−60	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 1 MΩ)	−100	−60	−100	−60	V
I_D @ T_C = 100°C	Continuous Drain Current	−7	−7	−6	−6	A
I_{DM}	Pulsed Drain Current	−30	−30	−25	−25	A
V_{GS}	Gate — Source Voltage	±20				V
P_D	Max. Power Dissipation	75 (See Fig. 11)				W
	Linear Derating Factor	0.6 (See Fig. 11)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH −30	−30	−25	−25	A
T_J T_{stg}	Operating and Storage Temperature Range	−55 to 150				°C

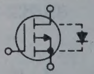
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRF9530 IRF9532	−100	—	—	V	V_{GS} = 0V
		IRF9531 IRF9533	−60	—	—	V	I_D = −1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	−2.0	—	−4.0	V	$V_{DS} = V_{GS}$, I_D = −1.0 mA
I_{GSS}	Gate — Body Leakage	ALL	—	—	−500	nA	V_{GS} = −20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	−0.1	−1.0	mA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	−0.2	−4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0V, T_J = 125°C
$I_{D\ (on)}$	On-State Drain Current	IRF9530 IRF9531	−12	—	—	A	V_{DS} = −25V, V_{GS} = −10V
		IRF9532 IRF9533	−10	—	—	A	
$R_{DS\ (on)}$	Static Drain-Source On State Resistance	IRF9530 IRF9531	—	0.25	0.30	Ω	V_{GS} = −10V, I_D = −4A
		IRF9532 IRF9533	—	0.30	0.40	Ω	
g_{fs}	Forward Transconductance	ALL	2.0	3.5	—	S (℧)	V_{DS} = −25V, I_D = −4A
C_{iss}	Input Capacitance	ALL	—	500	700	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	200	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	—	30	60	ns	I_D = −4A, E_1 = 0.5 BV_{DSS} (See Fig. 13) T_J = 125°C (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	70	140	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	—	70	140	ns	
t_f	Fall Time	ALL	—	70	140	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	—	—	1.0	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_{DR}	Continuous Reverse Drain Current	IRF9530, 9531	—	—	−7.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF9532, 9533	—	—	−6.0		
I_{DRM}	Pulsed Reverse Drain Current	IRF9530, 9531	—	—	−30	A	
		IRF9532, 9533	—	—	−25		
V_{SD}	Diode Forward Voltage	IRF9530, 9531	—	—	−5.5	V	T_J = 25°C, $I_F = I_{DRM}$, V_{GS} = 0V
		IRF9532, 9533	—	—	−5.3		
t_{rr}	Reverse Recovery Time	ALL	—	300	—	ns	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.0	—	μC	T_J = 150°C, $I_F = I_{DRM}$, dI_F/dt = 100 A/μs

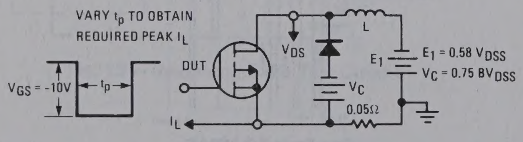


Fig. 1 — Clamped Inductive Test Circuit

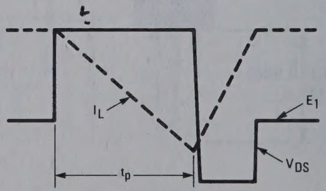


Fig. 2 — Clamped Inductive Waveform

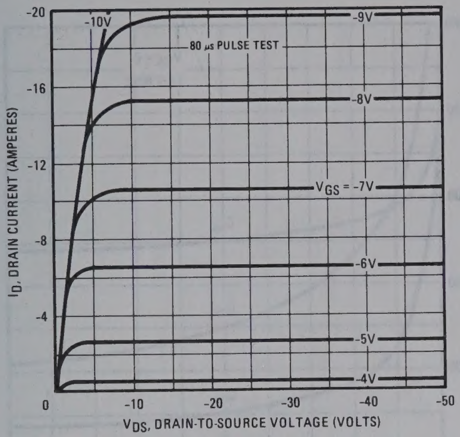


Fig. 3 — Typical Output Characteristics

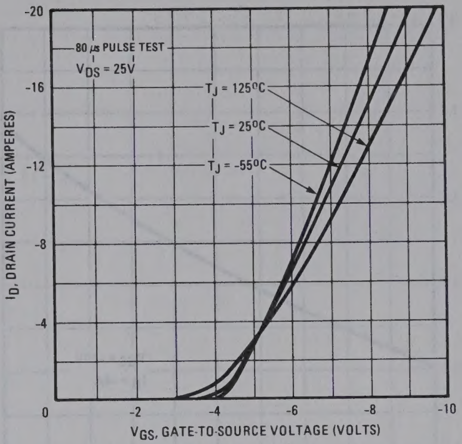


Fig. 4 — Typical Transfer Characteristics

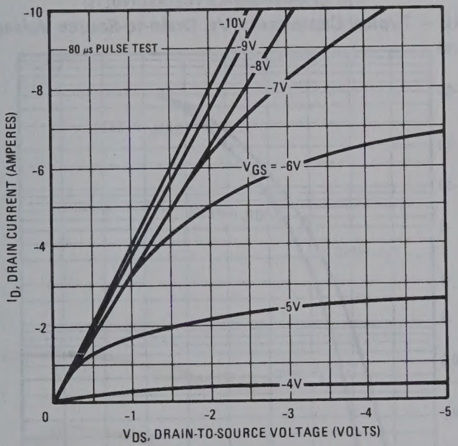


Fig. 5 — Typical Saturation Characteristics (IRF9530, IRF9531)

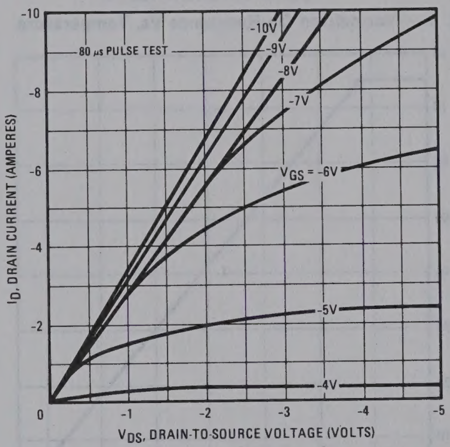


Fig. 6 — Typical Saturation Characteristics (IRF9532, IRF9533)

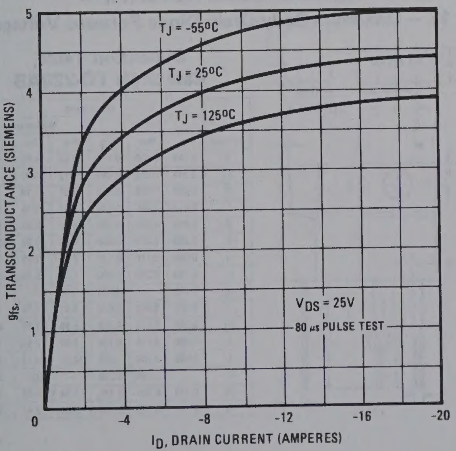


Fig. 7 — Typical Transconductance Vs. Drain Current

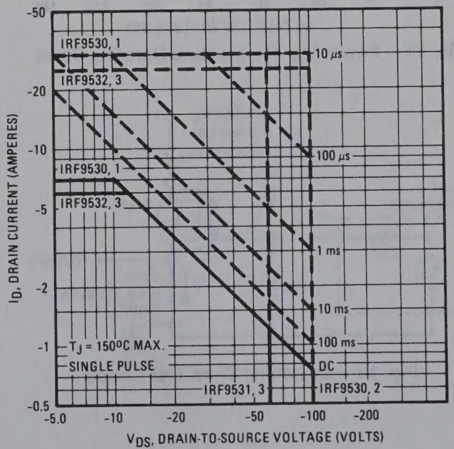


Fig. 8 — Maximum Safe Operating Area

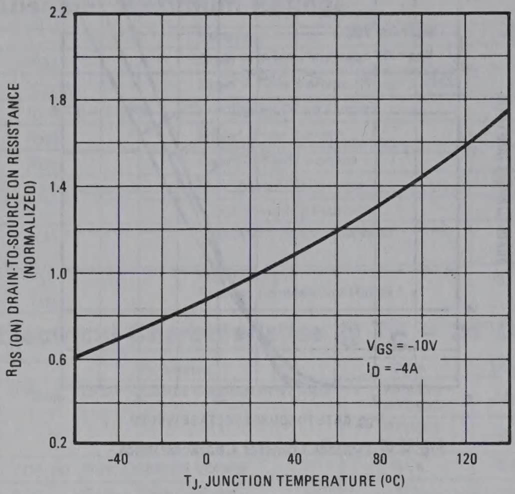


Fig. 9 — Normalized On-Resistance Vs. Temperature

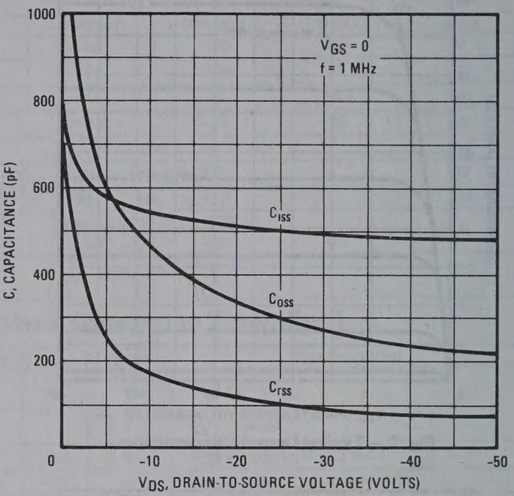


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

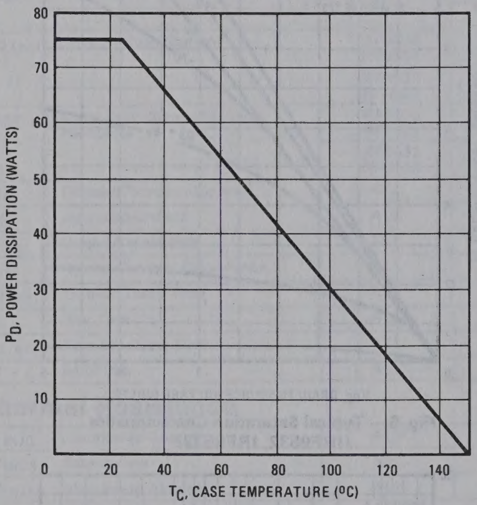


Fig. 11 — Power Vs. Temperature Derating Curve

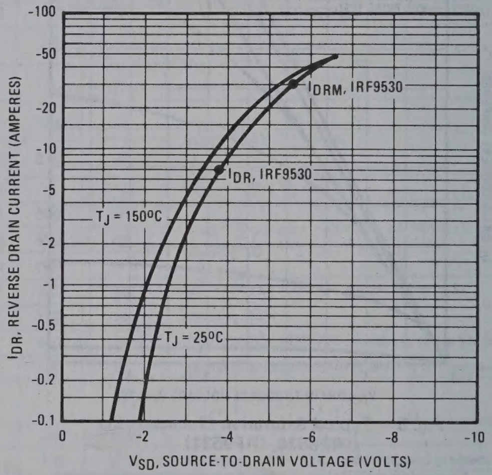


Fig. 12 — Maximum Body-Drain Diode Forward Voltage

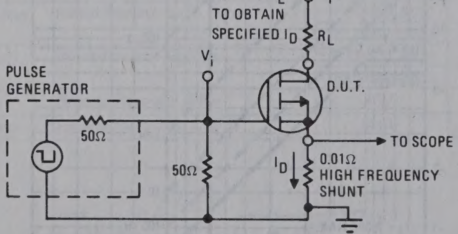
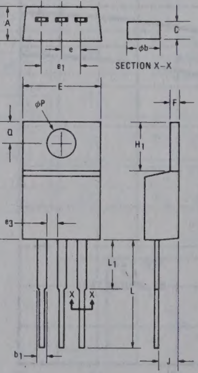


Fig. 13 — Switching Time Test Circuit



Dimension Table, Case Style TO-220AB

Symbol	Dimensions					
	Inches			Millimeters		
	Min.	Max.	Typ.	Min.	Max.	Typ.
A	0.140	0.190	0.175	3.56	4.82	4.45
b_1	0.045	0.070	0.050	1.15	1.77	1.27
φb	0.020	0.045	0.032	0.51	1.14	0.81
C	0.012	0.045	0.018	0.31	1.14	0.46
D	0.560	0.650	0.590	14.23	16.51	14.99
E	0.380	0.420	0.400	9.66	10.66	10.16
e	0.090	0.110	0.100	2.29	2.79	2.54
e_1	0.190	0.210	0.200	4.83	5.33	5.08
e_3	0.045	–	0.050	1.15	–	1.27
F	0.020	0.055	0.050	0.51	1.39	1.27
H_1	0.230	0.270	0.248	5.85	6.85	6.30
J	0.080	0.115	0.105	2.04	2.92	2.67
L	0.500	0.580	0.550	12.70	14.73	13.98
L_1	–	0.250	0.230	–	6.35	5.84
φP	0.139	0.161	0.145	3.54	4.08	3.68
Q	0.100	0.135	0.108	2.54	3.42	2.74

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Kierulff Electronics
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Hingham, MA 02043
Sager Electrical
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60 Research Road
Phone: (617) 749-6700

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2280 S. Industrial Highway
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Livonia, MI 48150
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TWX: 810-243-4026

Schweber Electronics
33540 Schoolcraft
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7402 Washington Avenue S.
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Edina, MN 55435
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Stark Electronics
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2550 Harley Drive
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St. Louis, MO 63132
Olive Electronics, Inc.
9910 Page Blvd.
Phone: (314) 426-4500

St. Louis, MO 63104
Van Sickle
Radio Elect.
2014 S. Seventh Street
Phone: (314) 621-5000

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Marshall-Wilshire
1111 Paulison Avenue
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TWX: 710-989-7052

Fairfield, NJ 07006
Kierulff Electronics
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Schweber Electronics
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Parts Company
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Summit Distributors
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Phone: (716) 887-3450

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Schweber Electronics
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TWX: 510-222-3660

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Phone: (704) 377-5413

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414 Hillsborough Street
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Stotts-Friedman
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Phone: (513) 298-5555

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Phone: (216) 248-8900

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REM Electronic Supply
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Radar Electronics
704 SE Washington
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Kierulff Electronics
14273 N.W. Science Park
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ALMO Electronic Corp.
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CAM/RPC Electronics
620 Alpha Drive, RIDC Park
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Schweber Electronics
10625 Richmond, Suite 100
Phone: (713) 784-3600

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Solid State Electronics
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2121 S. 3600 West
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Virginia Radio Supply
715 Henry Avenue
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B-1020 Brussels
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